



IN THE U.S. PATENT AND TRADEMARK OFFICE

In re patent application of

K. Hayashi

Serial No.: 09/916,529

Group Art Unit: 2652

Filed: July 30, 2001

Examiner: Unknown

For: MAGNETO-RESISTANCE EFFECT ELEMENT, MAGNETO-RESISTANCE EFFECT HEAD, MAGNETO-RESISTANCE TRANSDUCER SYSTEM, AND MAGNETIC STORAGE SYSTEM

Assistant Commissioner for Patents
Washington, D.C. 20231

SUBMISSION OF FORMAL DRAWINGS

Sir:

Submitted herewith are fifty-one (51) sheets of formal drawings comprising figures 1-108 for the above-identified patent application. Please substitute the formal drawings for the drawings which were filed with the application.

Respectfully submitted,

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Reg. No.: 32,635

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(703)712-5000

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FIG. 1 (PRIOR ART)

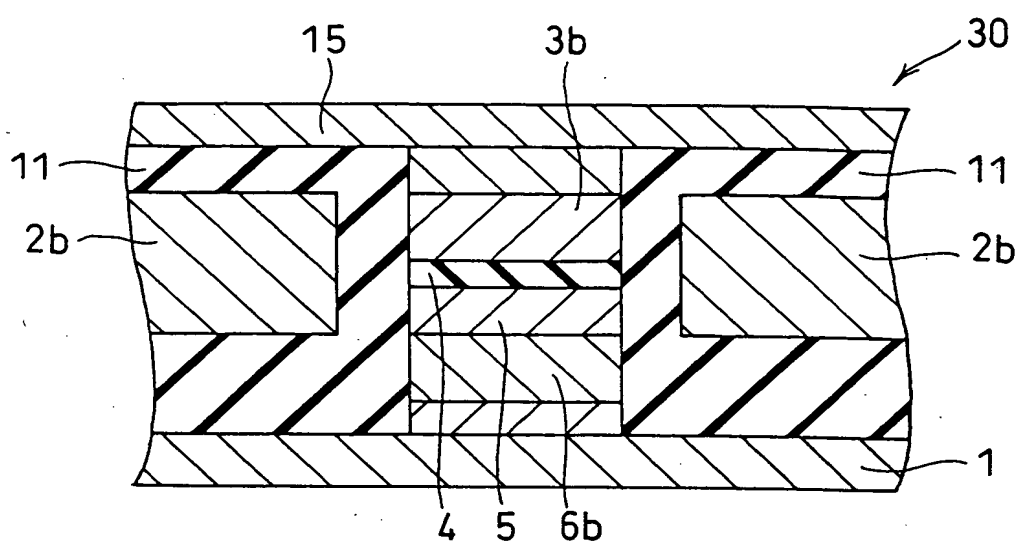


FIG. 2 (PRIOR ART)

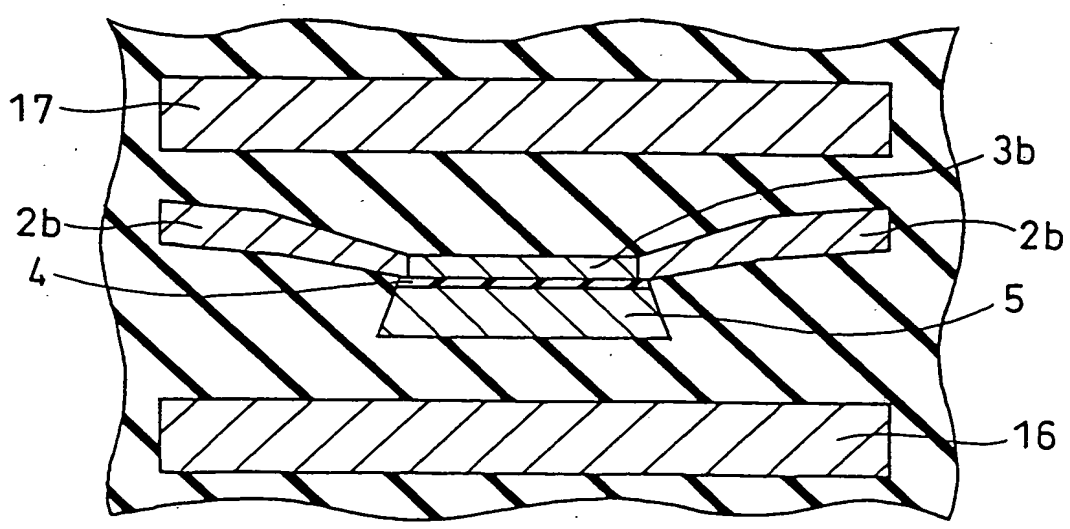


FIG. 3 (PRIOR ART)

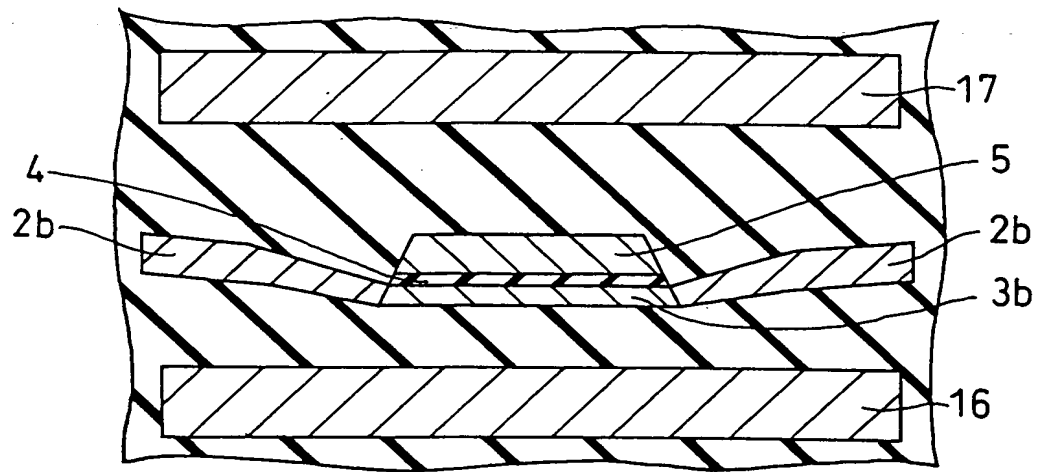


FIG. 4

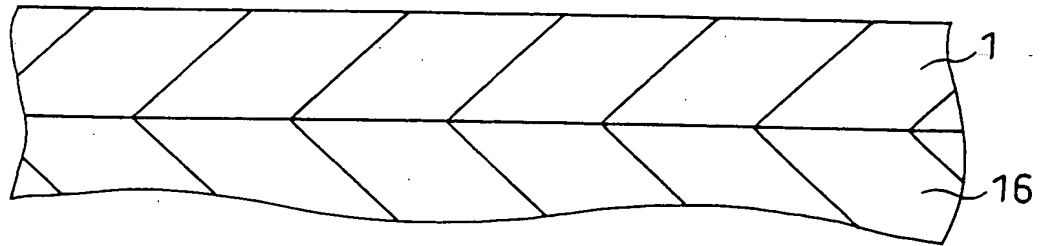


FIG. 5

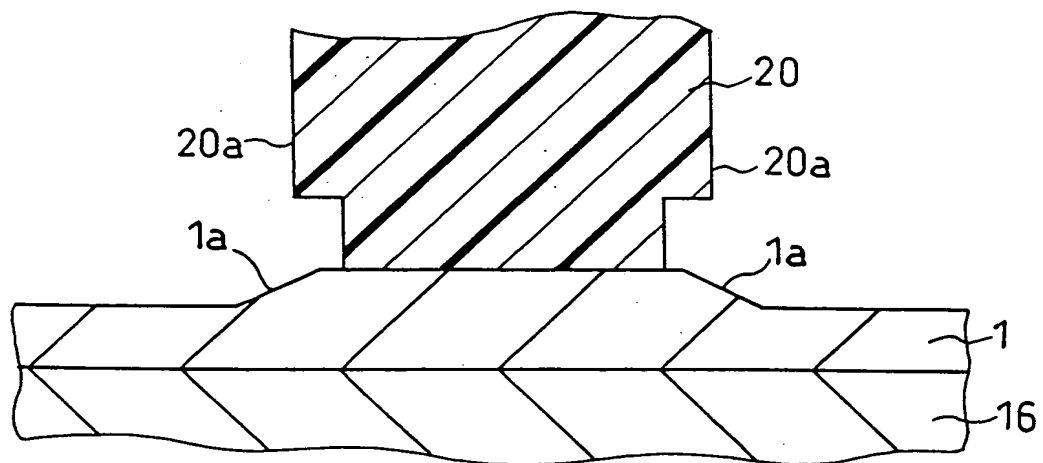


FIG. 6

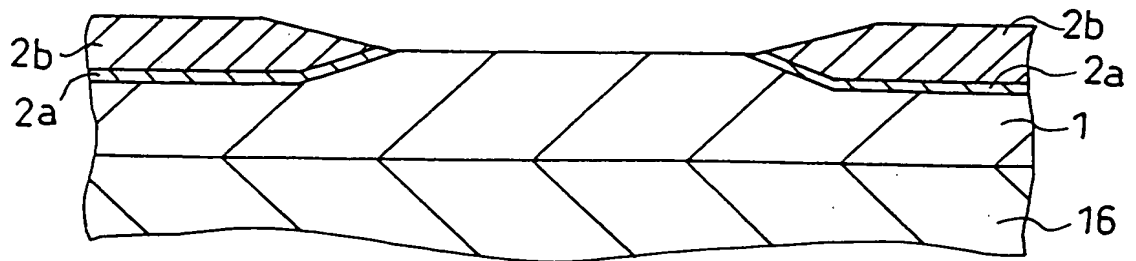


FIG. 7

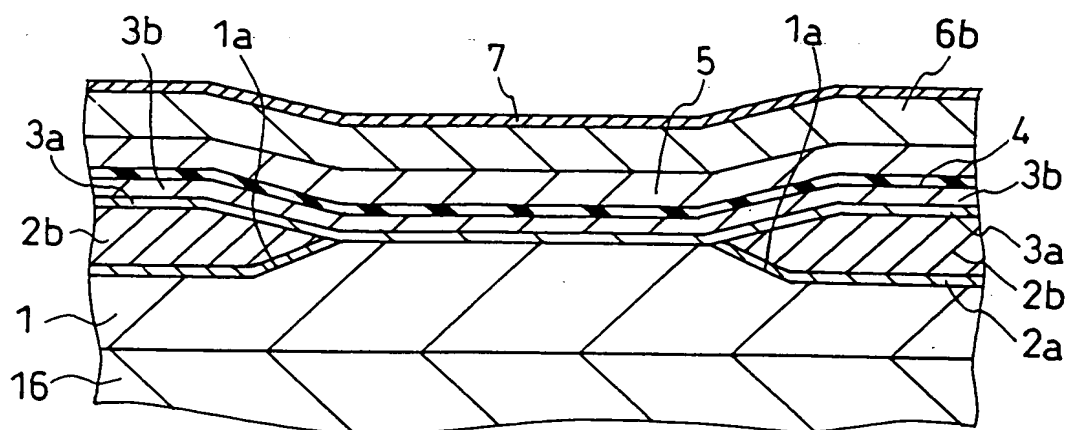


FIG. 8

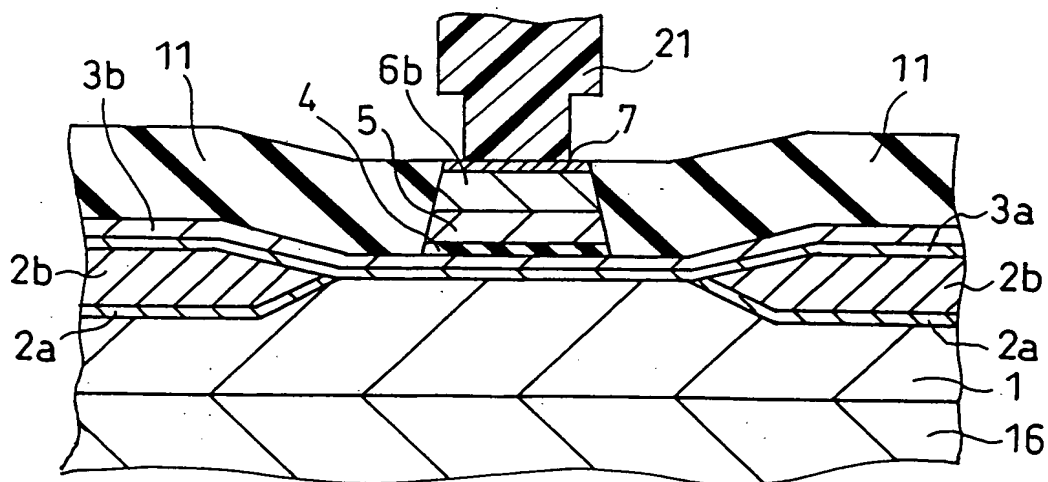


FIG. 9

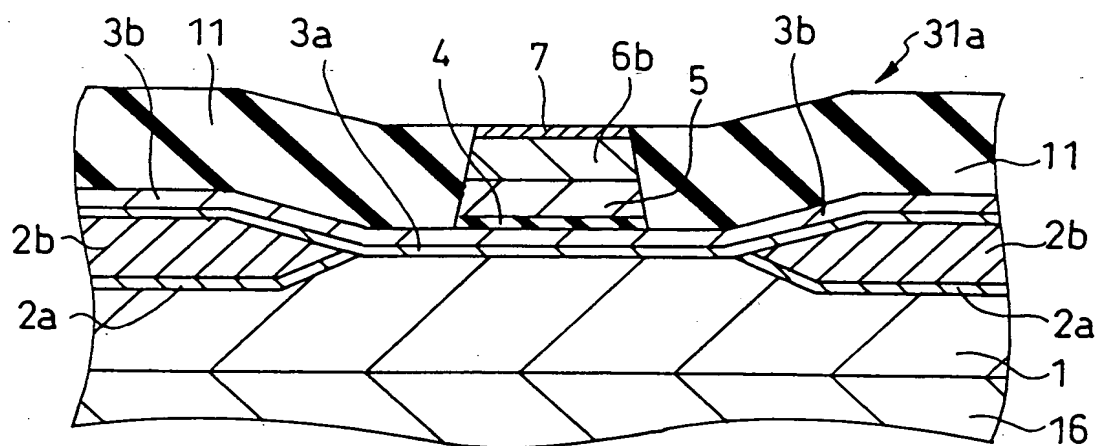


FIG. 10

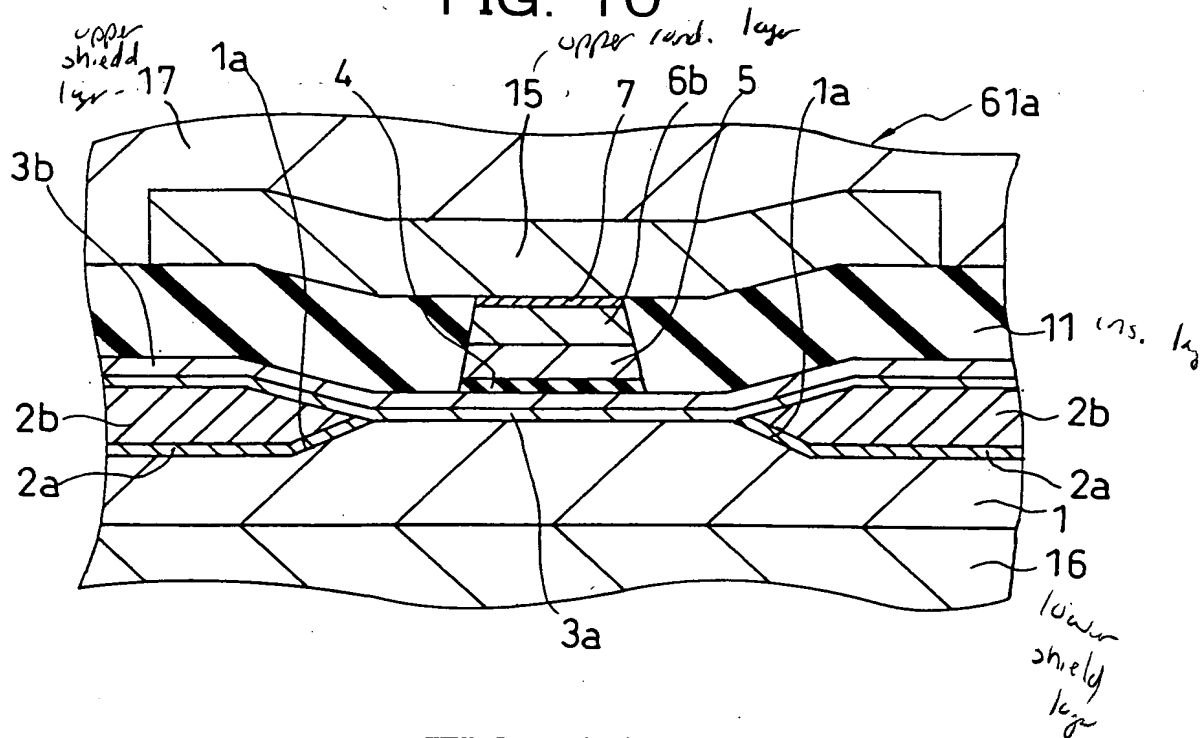


FIG. 11

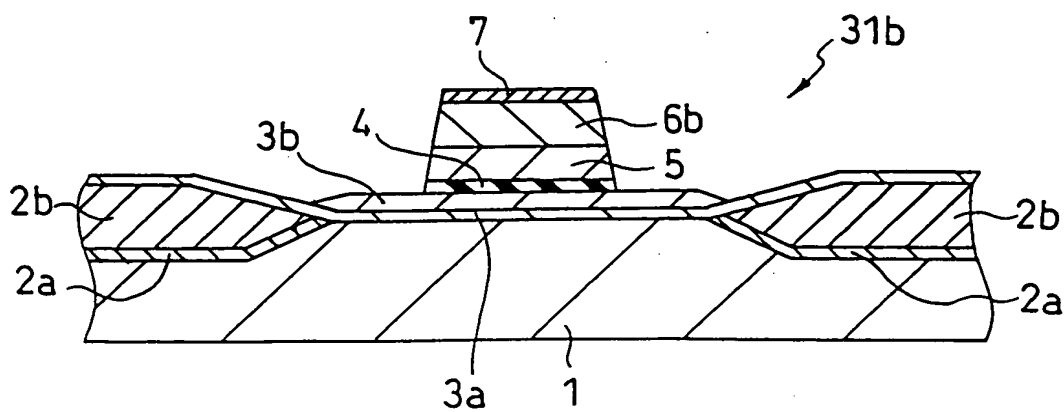


FIG. 12

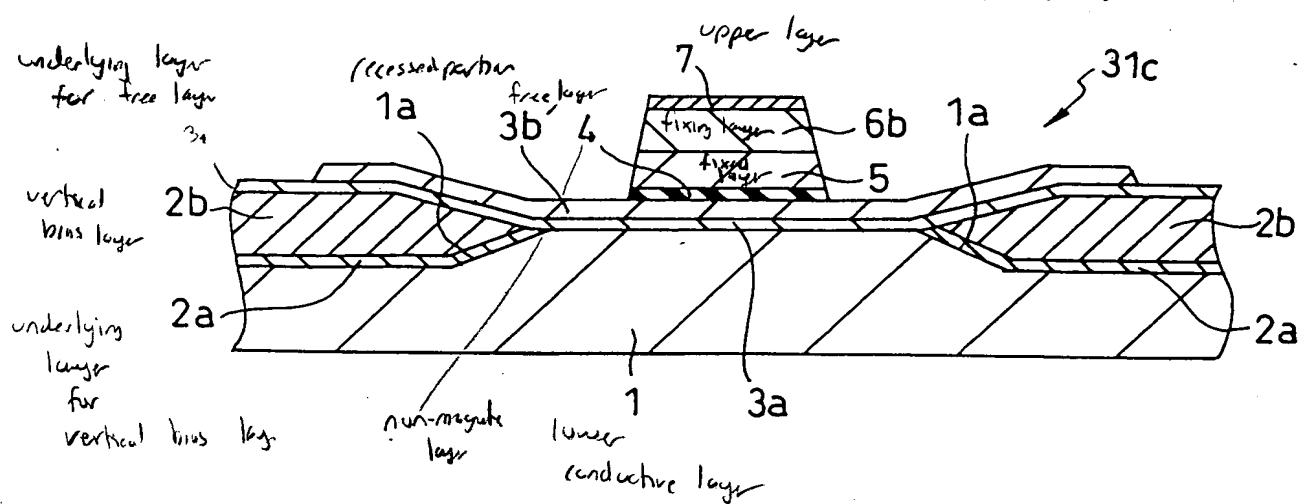


FIG. 13

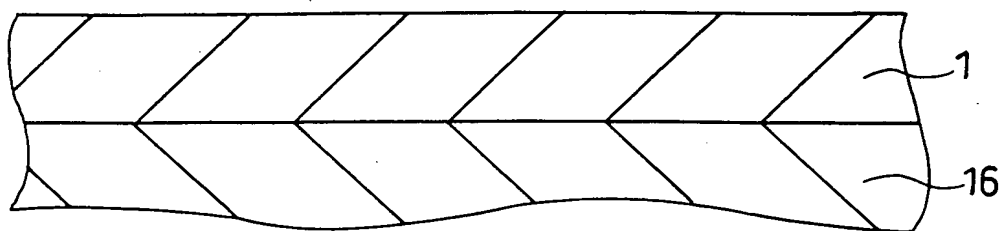


FIG. 14

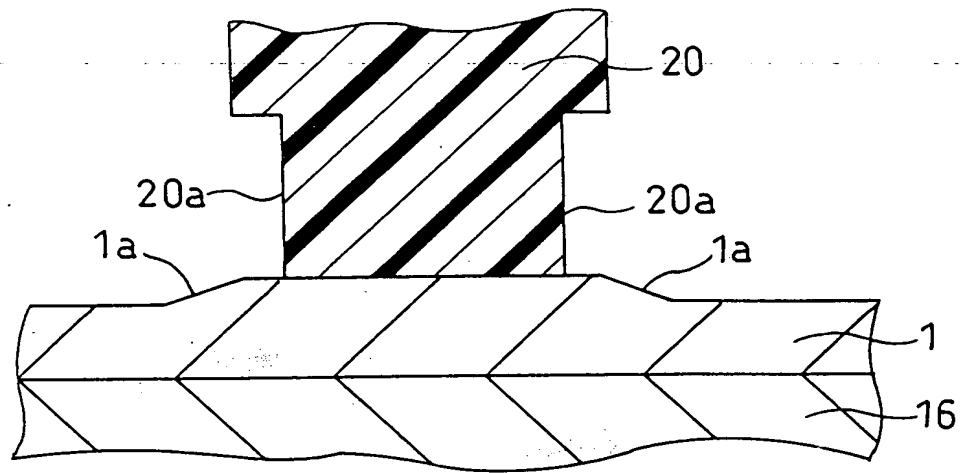


FIG. 15

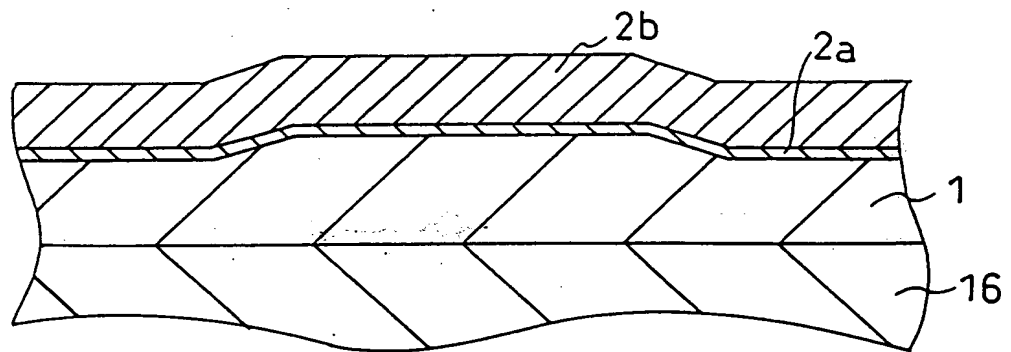


FIG. 16

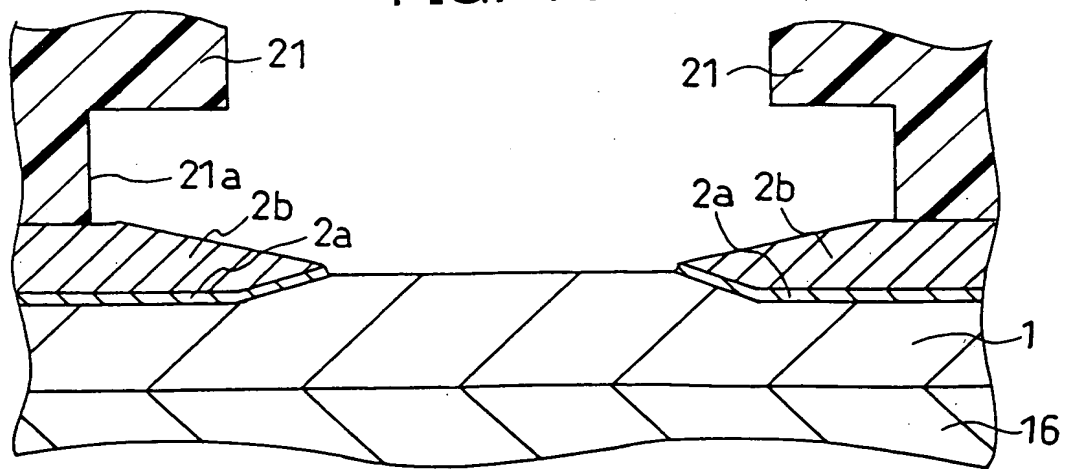


FIG. 17

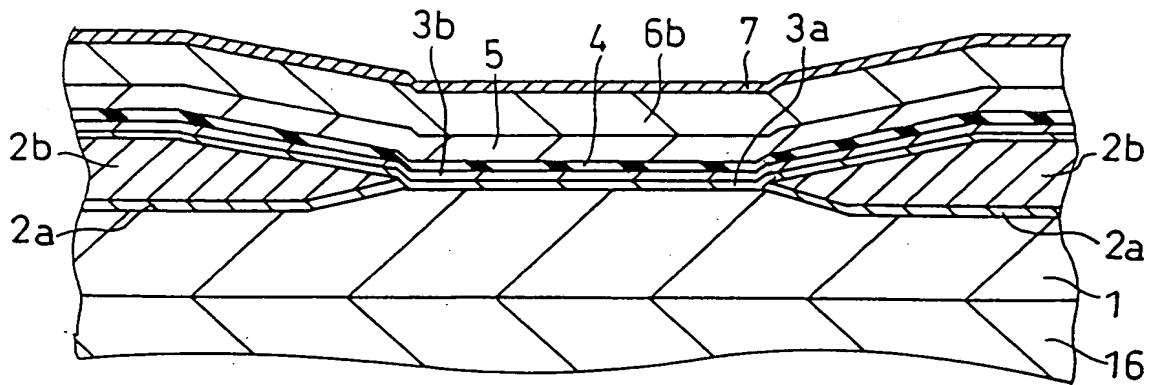


FIG. 18

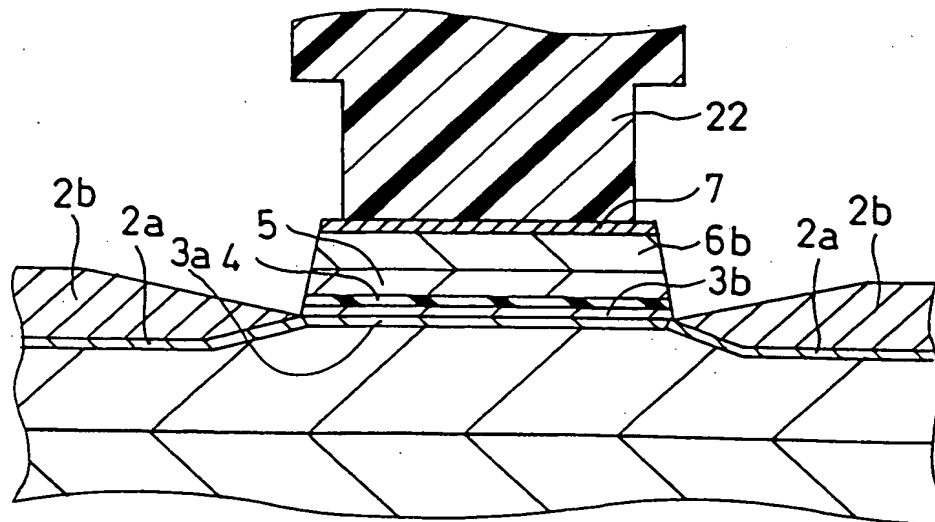


FIG. 19

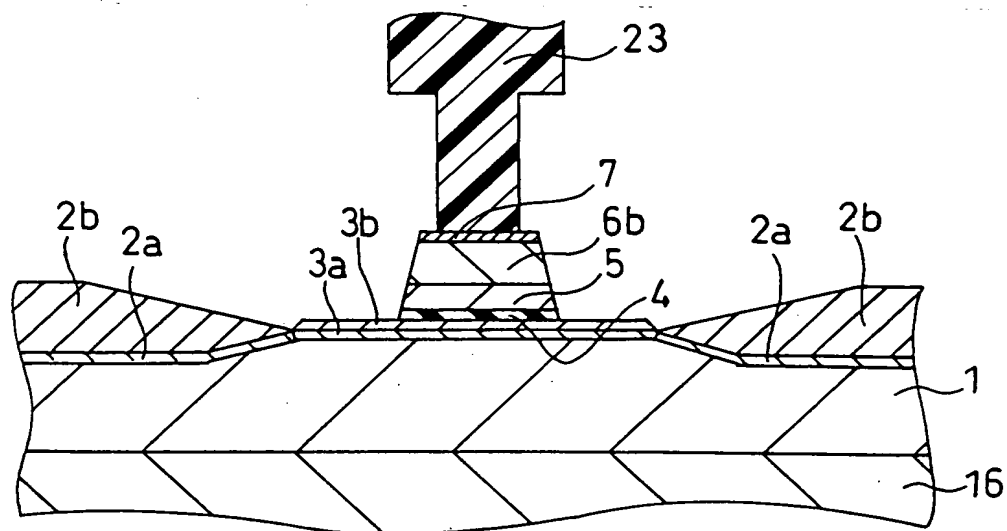


FIG. 20

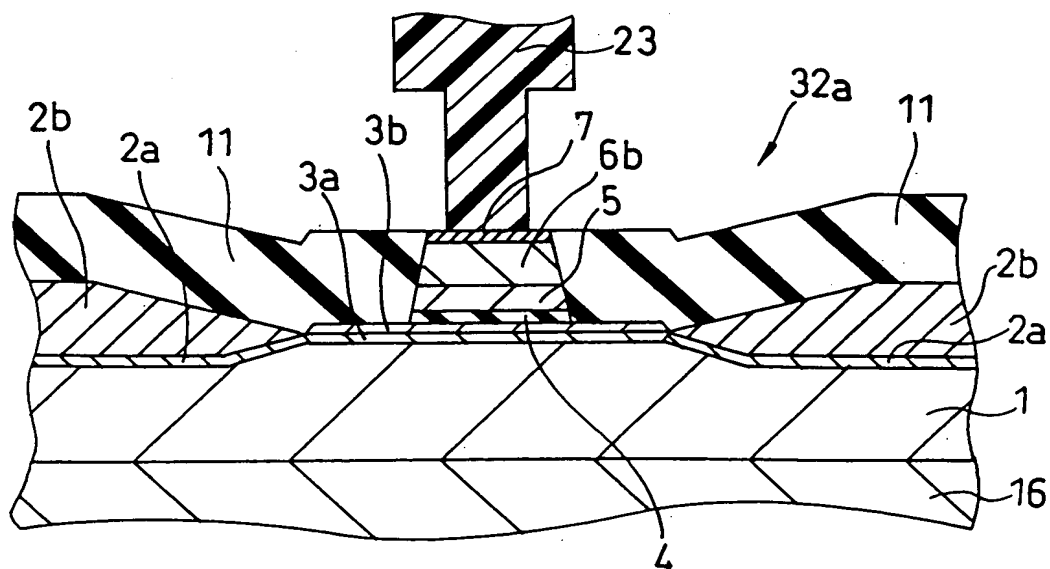


FIG. 21

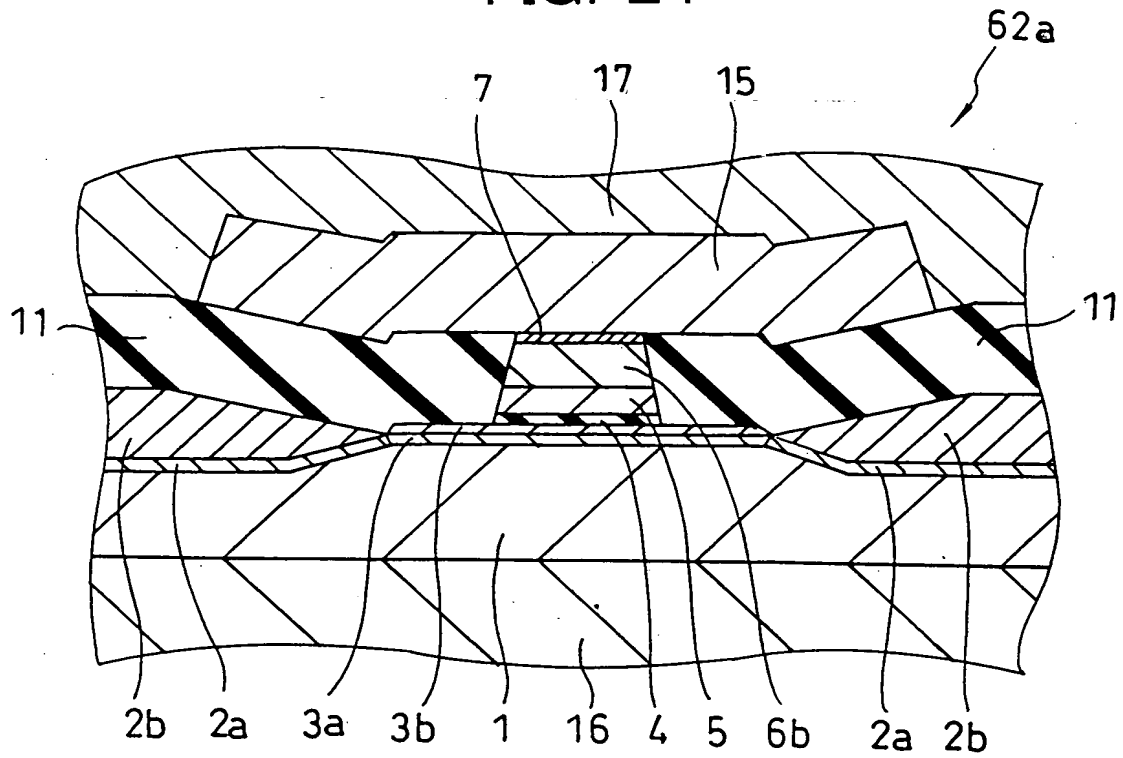


FIG. 22

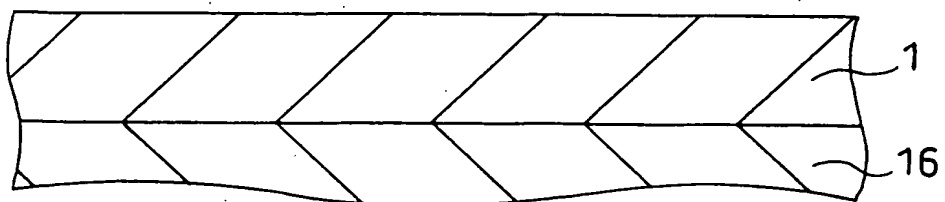


FIG. 23

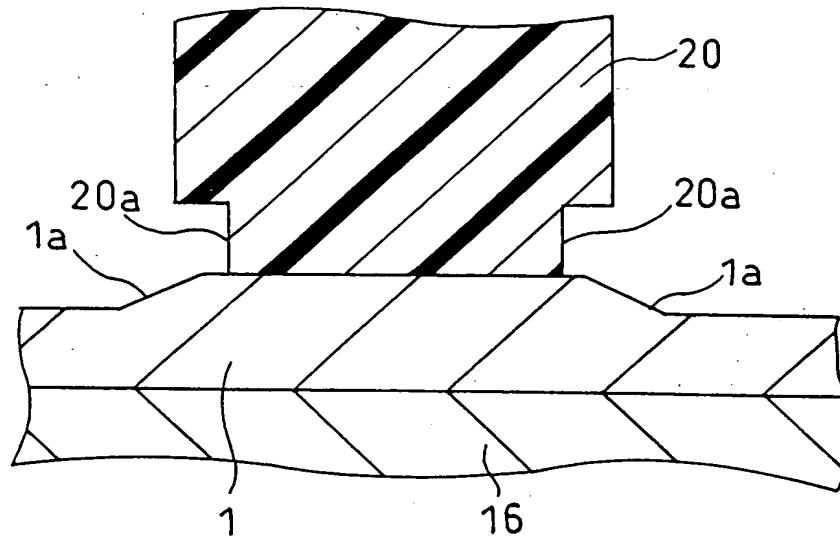


FIG. 24

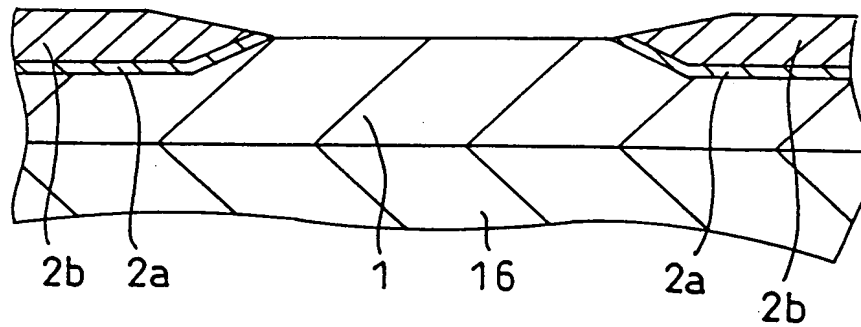


FIG. 25

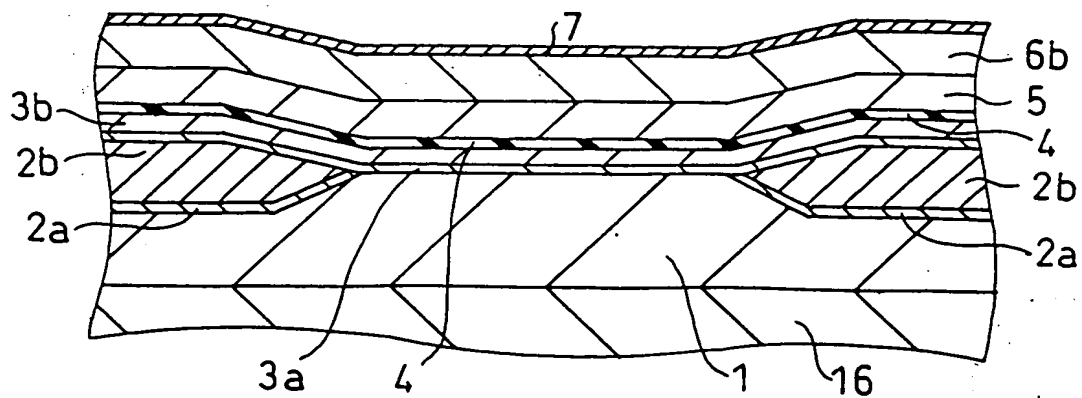


FIG. 26

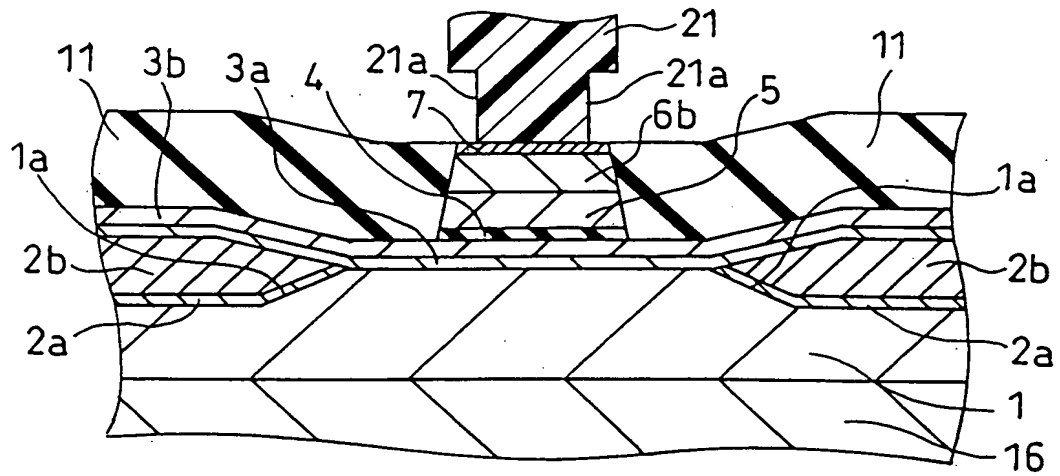


FIG. 27

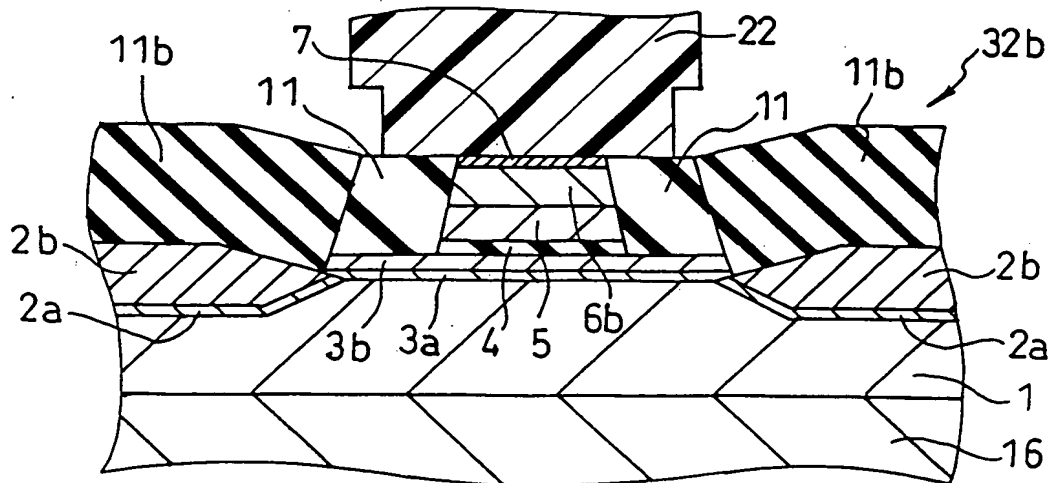


FIG. 28

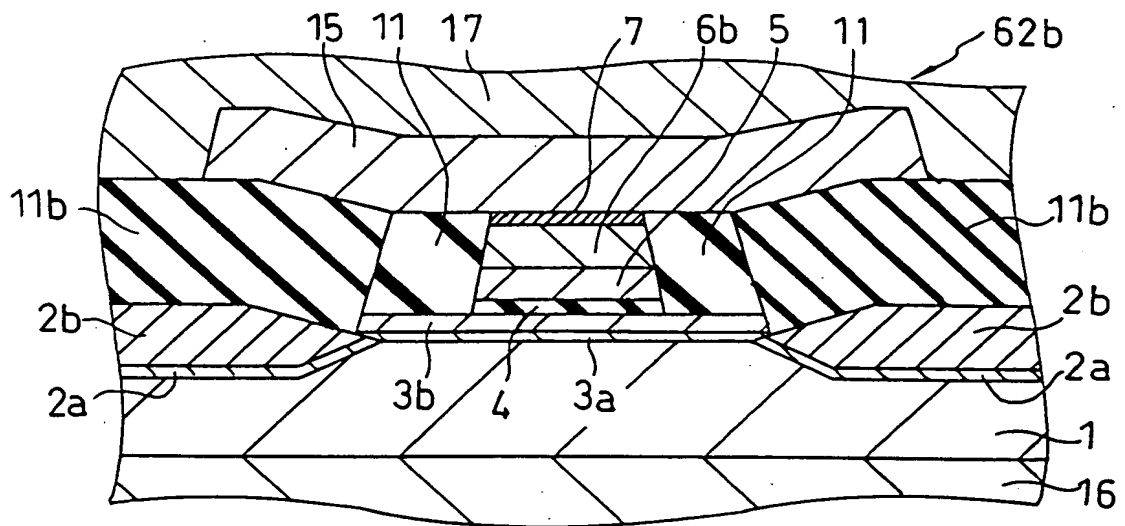


FIG. 29

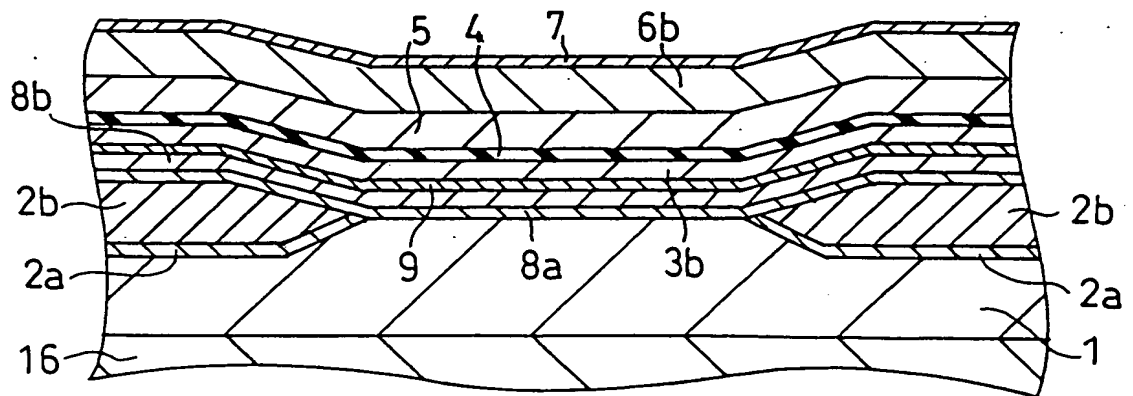


FIG. 30

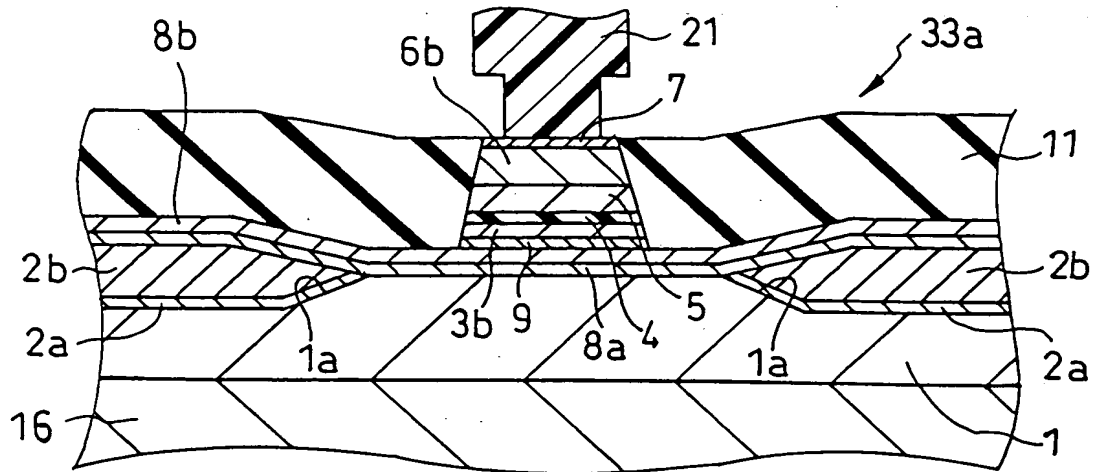


FIG. 31

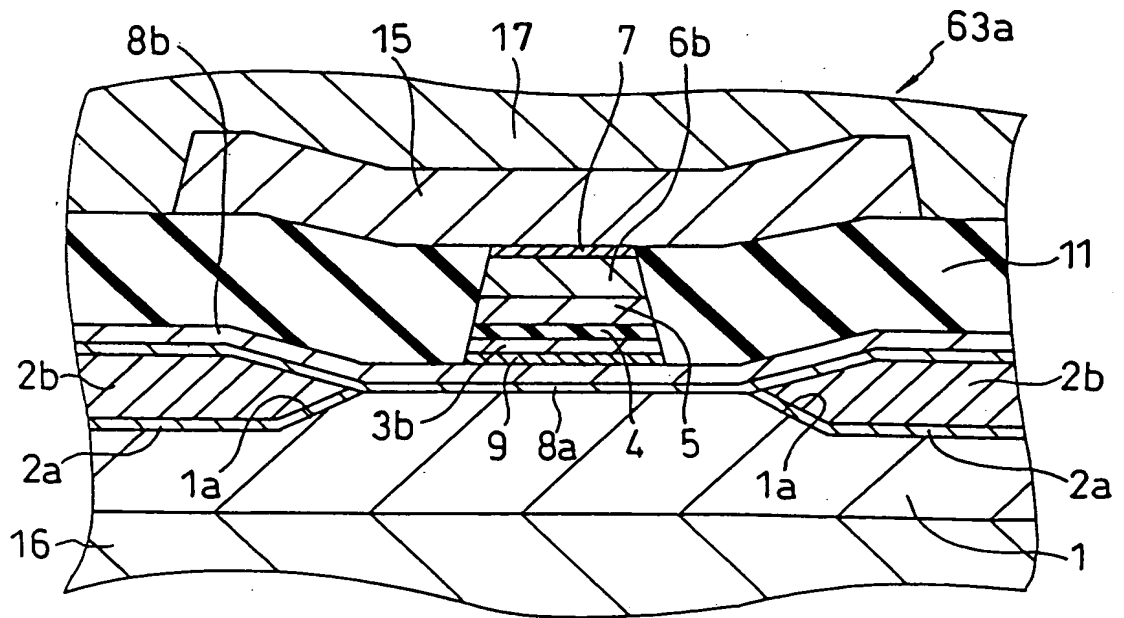


FIG. 32

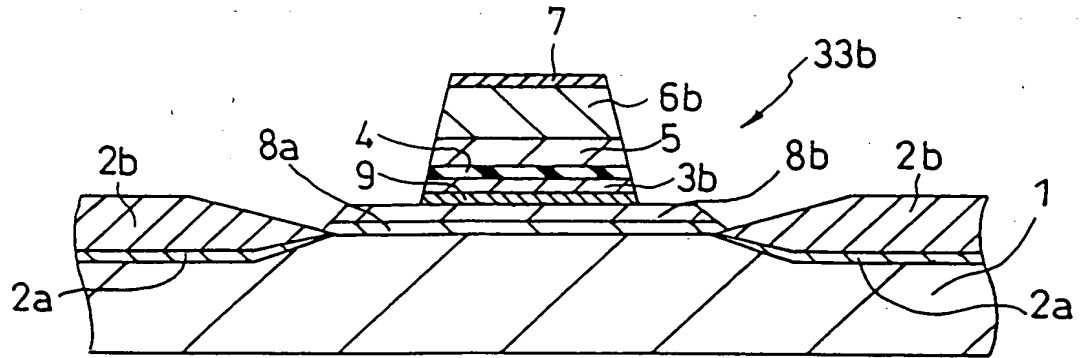


FIG. 33

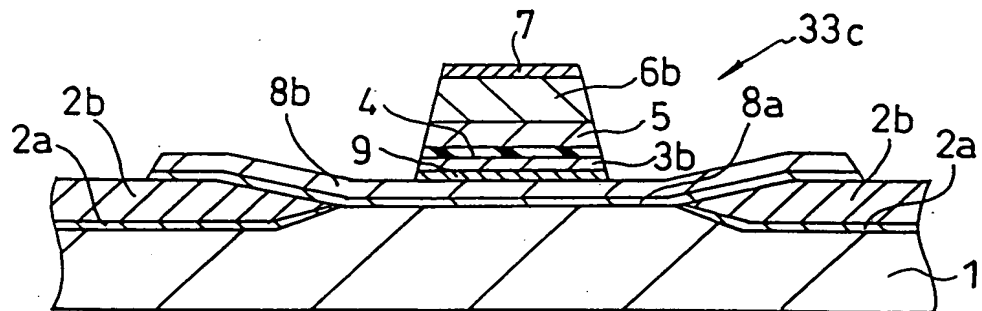


FIG. 34

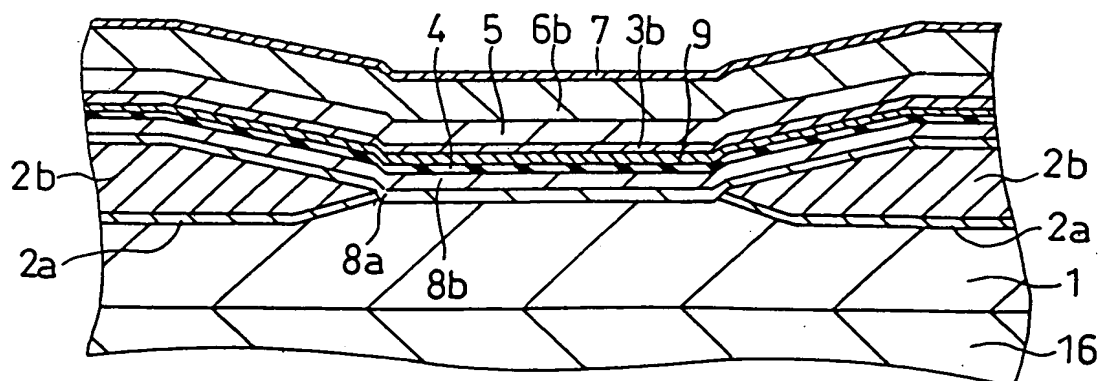


FIG. 35

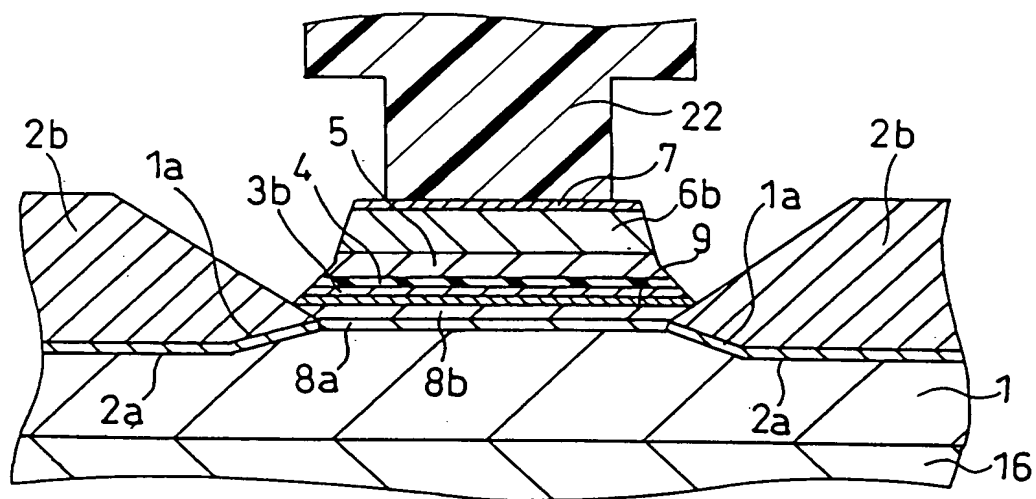


FIG. 36

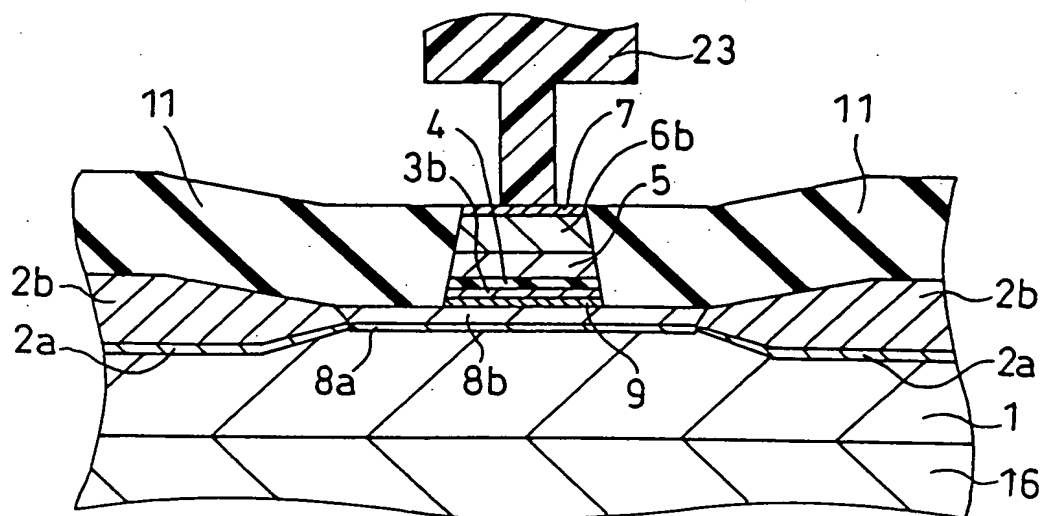


FIG. 37

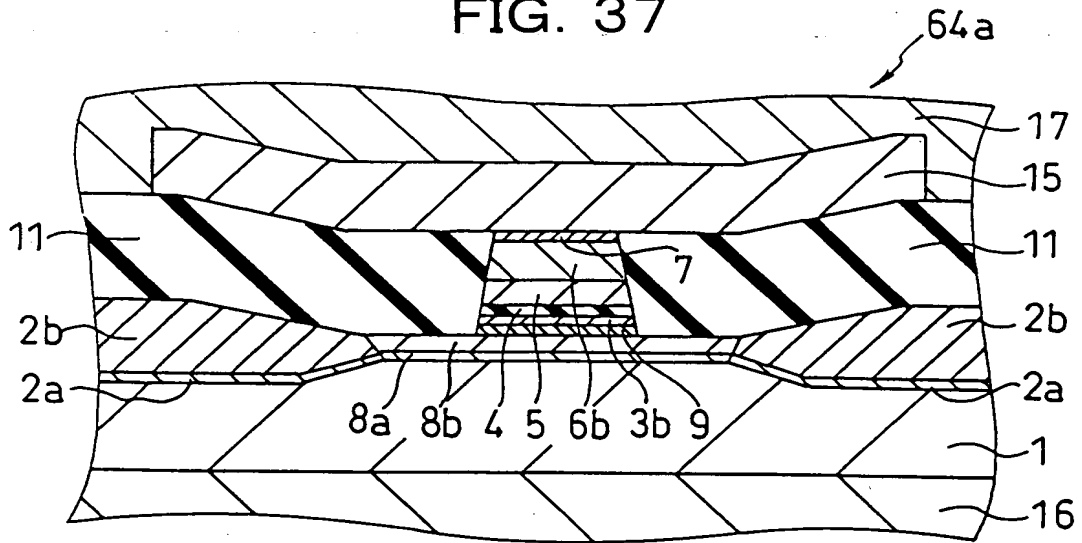


FIG. 38

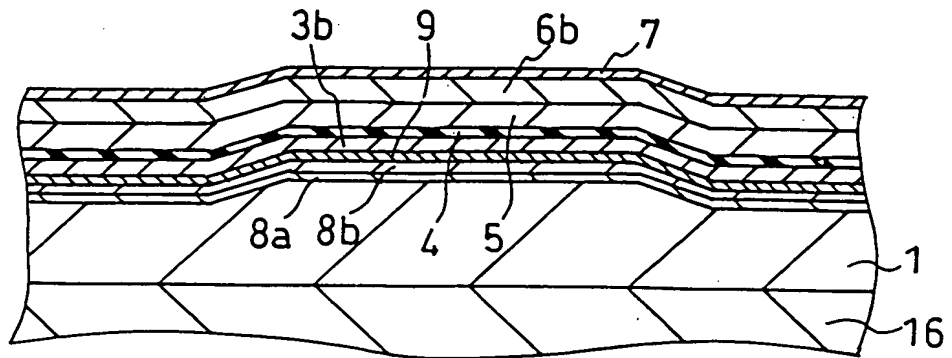


FIG. 39

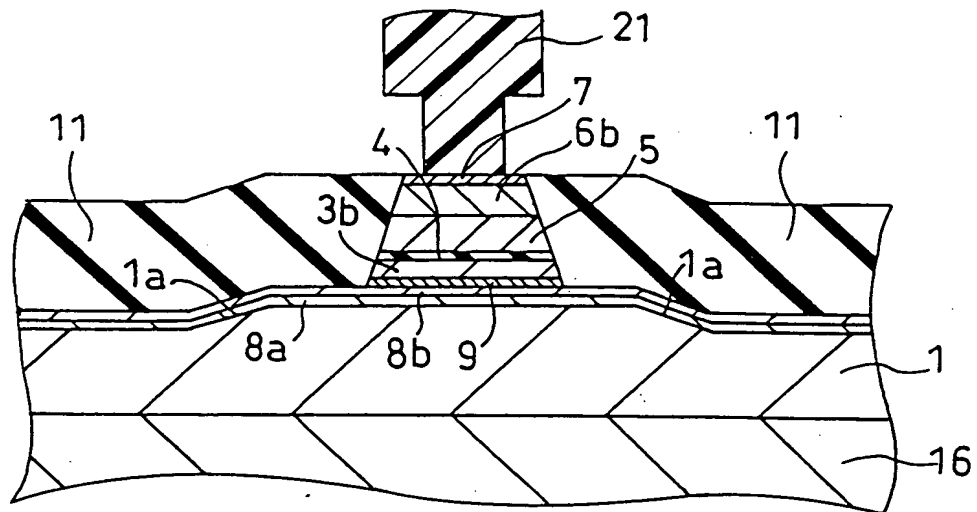


FIG. 40

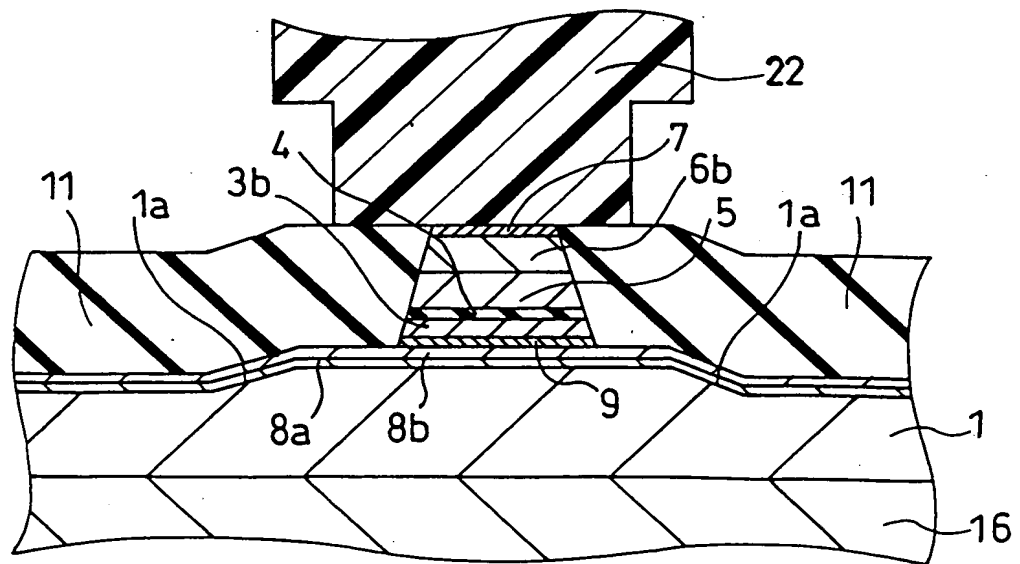


FIG. 41

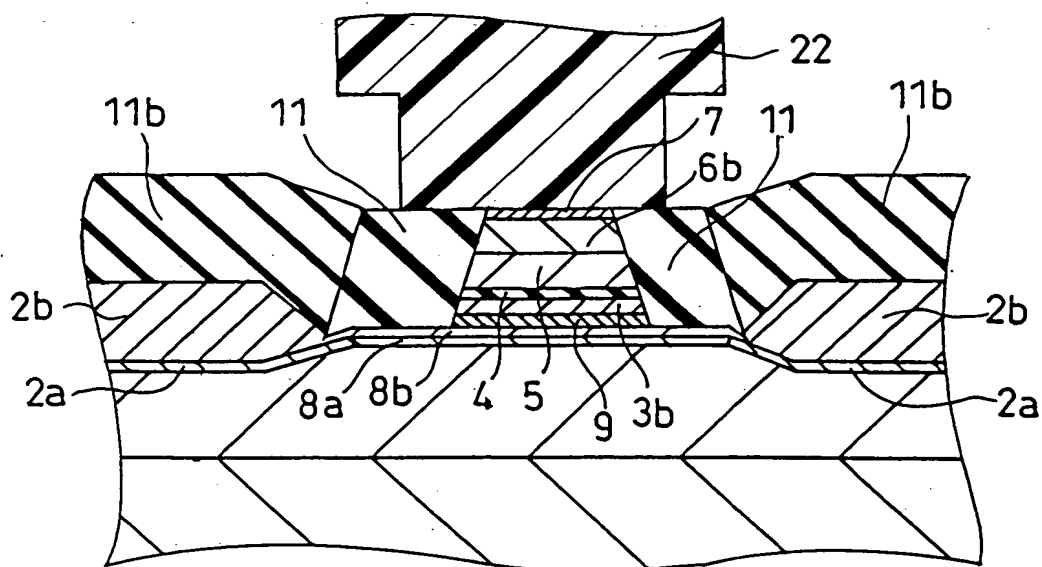


FIG. 42

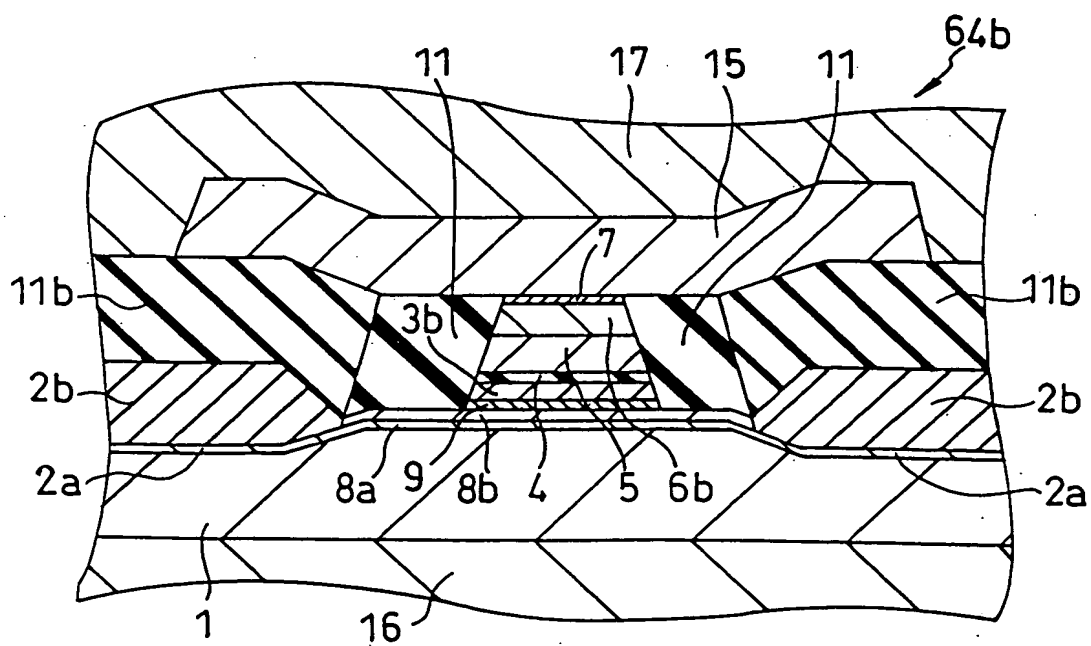


FIG. 43

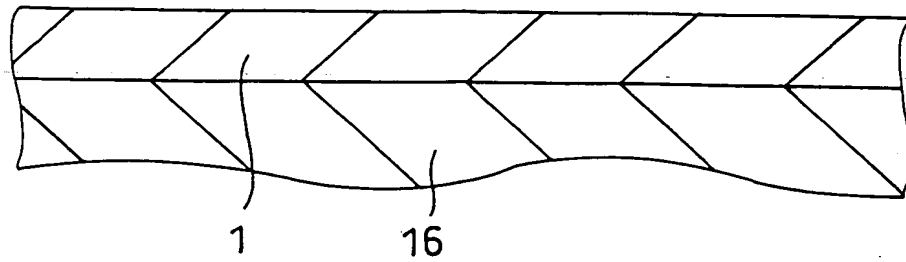


FIG. 44

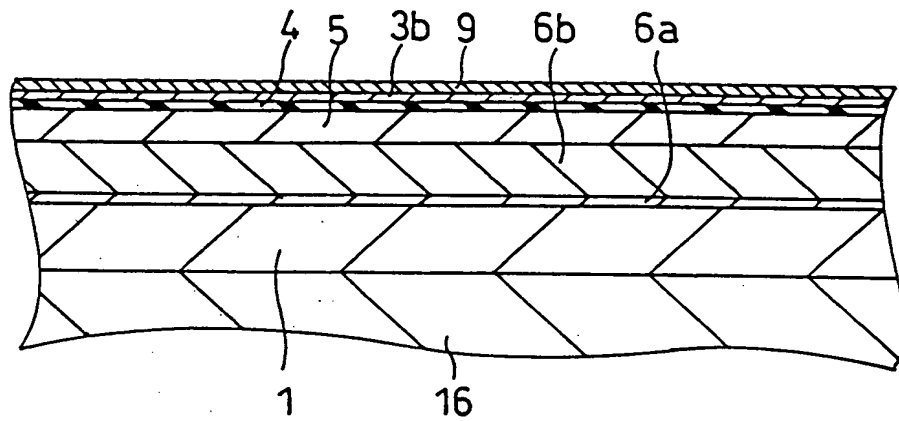


FIG. 45

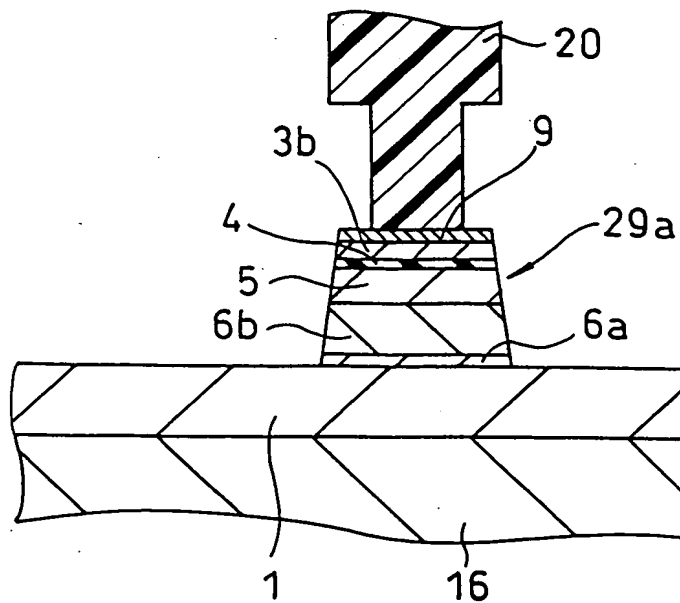


FIG. 46

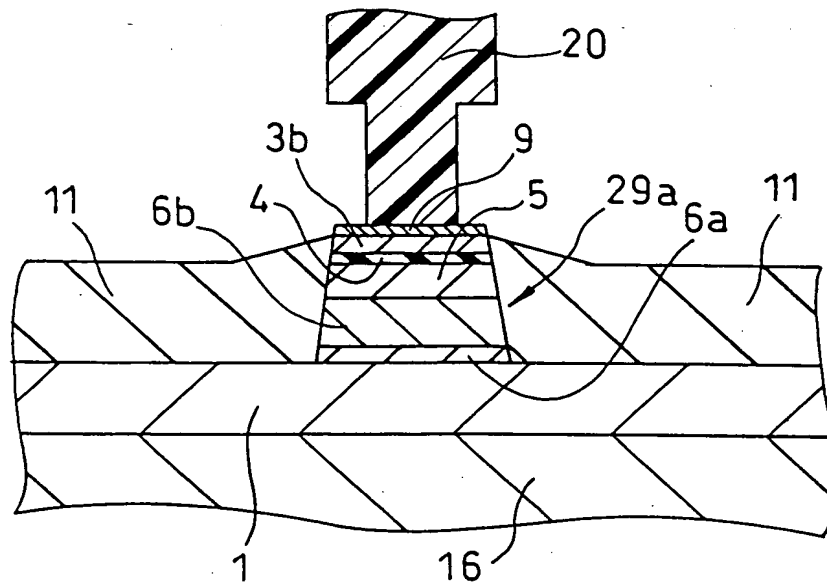


FIG. 47

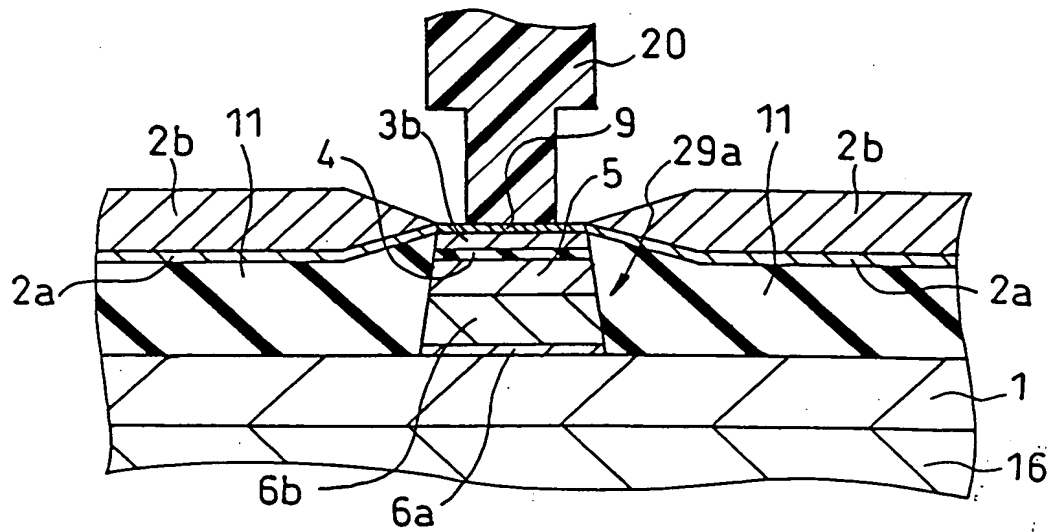


FIG. 48

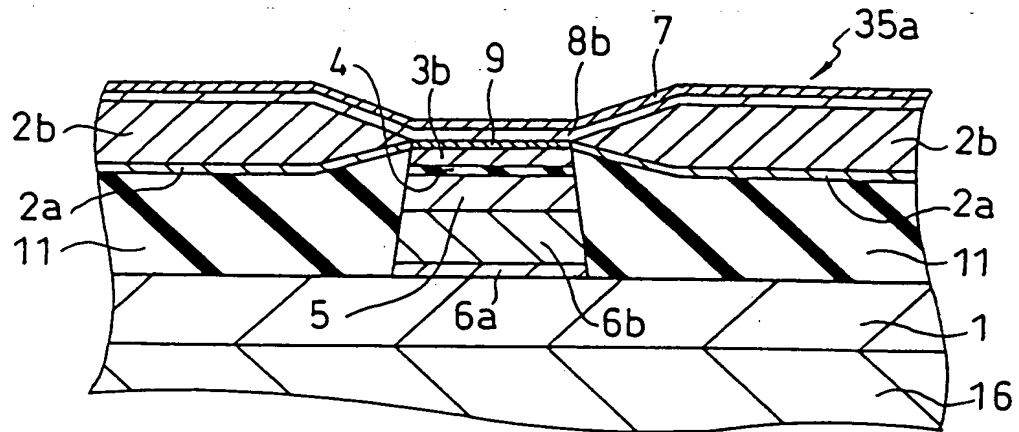


FIG. 49

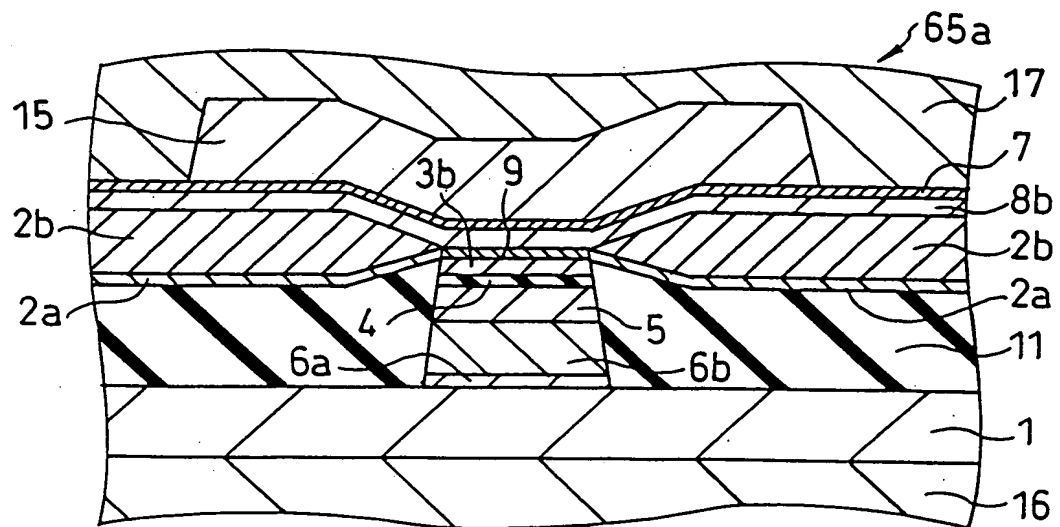


Fig. 1 is a cross-sectional view of a semiconductor device. The device consists of a substrate 1 with layers 6a and 6b. A central region 5 contains a series of V-shaped structures 4. The top surface is covered by layers 2a and 2b. A central channel 7 is formed between the V-shaped structures. Other labels include 3b, 8b, 9, and 11.

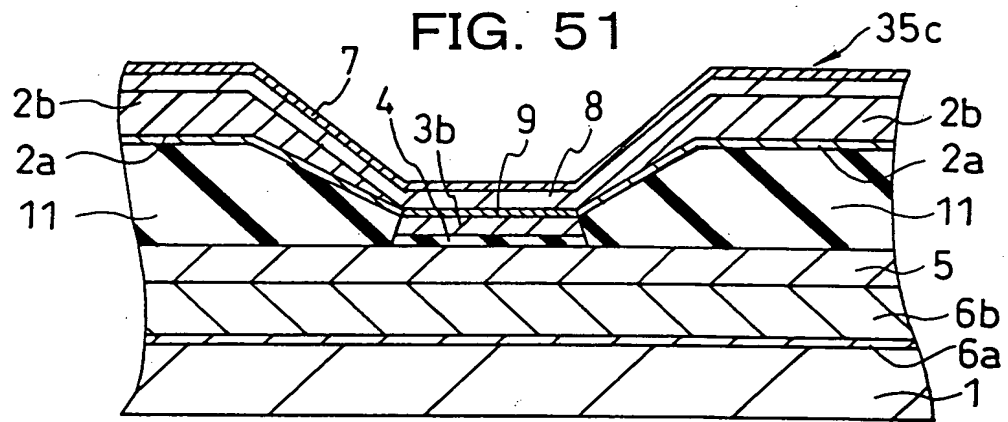
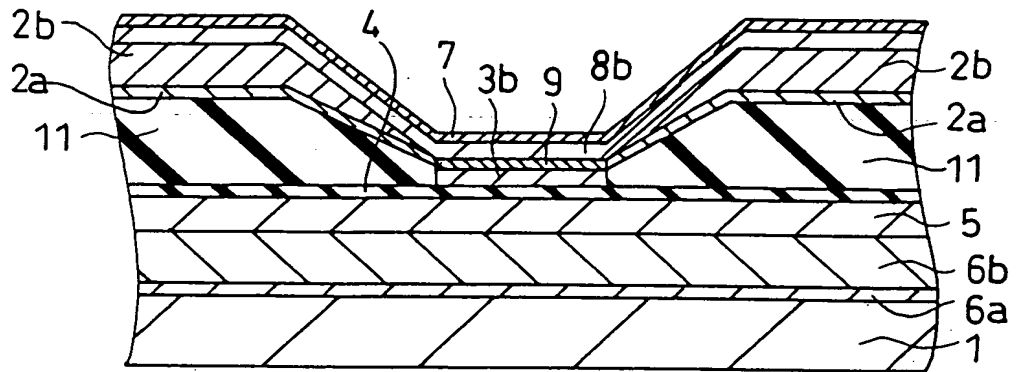


FIG. 52

A cross-sectional view of a semiconductor device. The device features a central channel region 3b and side regions 2a, 2b, 3a, 3b, 4, 5, 6a, 6b, 7, 8b, 9, 11, 35d, and 1. The channel region 3b is defined by a gate stack 4 and a source/drain region 5. The side regions 2a and 2b are adjacent to the channel region. The regions 3a and 3b are located on the sides of the channel region. The regions 4 and 5 are located on the top and bottom of the channel region. The regions 6a and 6b are located on the sides of the channel region. The regions 7 and 8b are located on the top and bottom of the channel region. The regions 9 and 11 are located on the sides of the channel region. The region 35d is located on the top of the channel region. The region 1 is located at the bottom of the device.

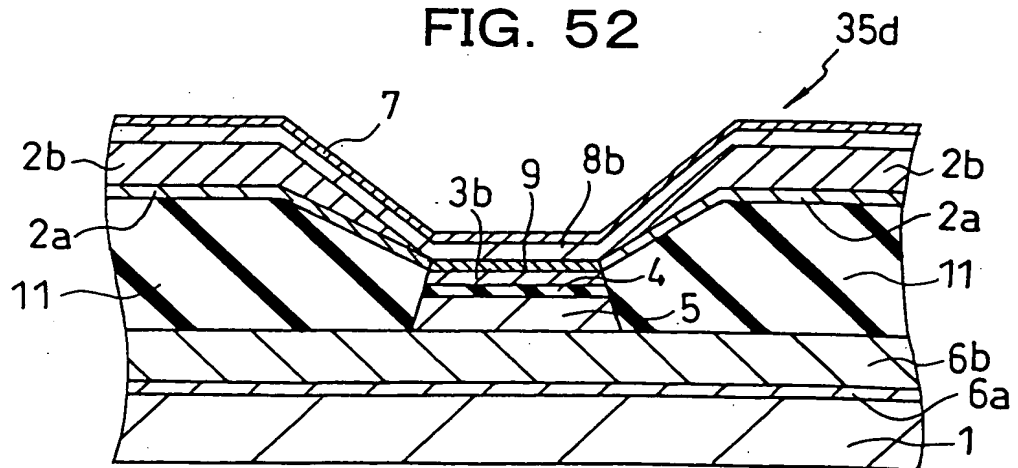


FIG. 53

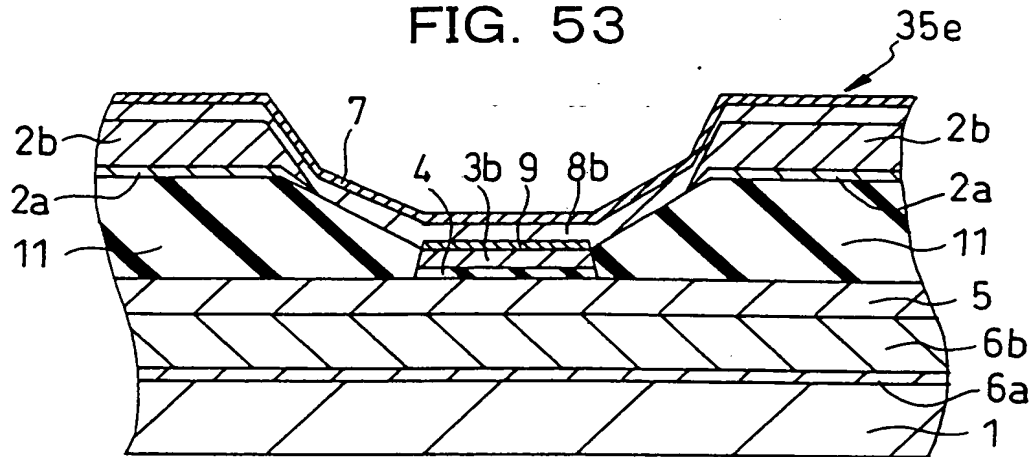


FIG. 54

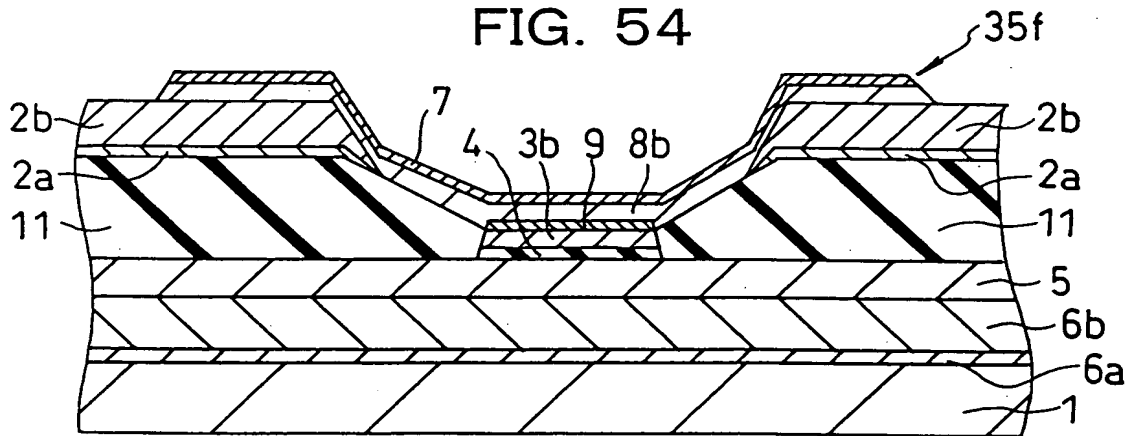


FIG. 55

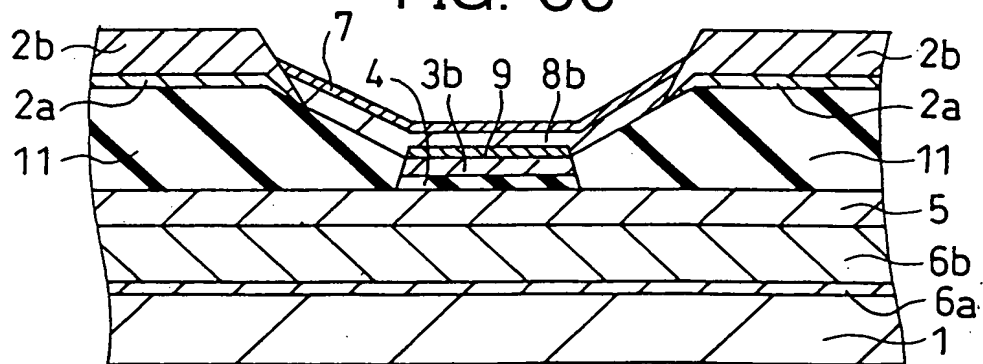


FIG. 56

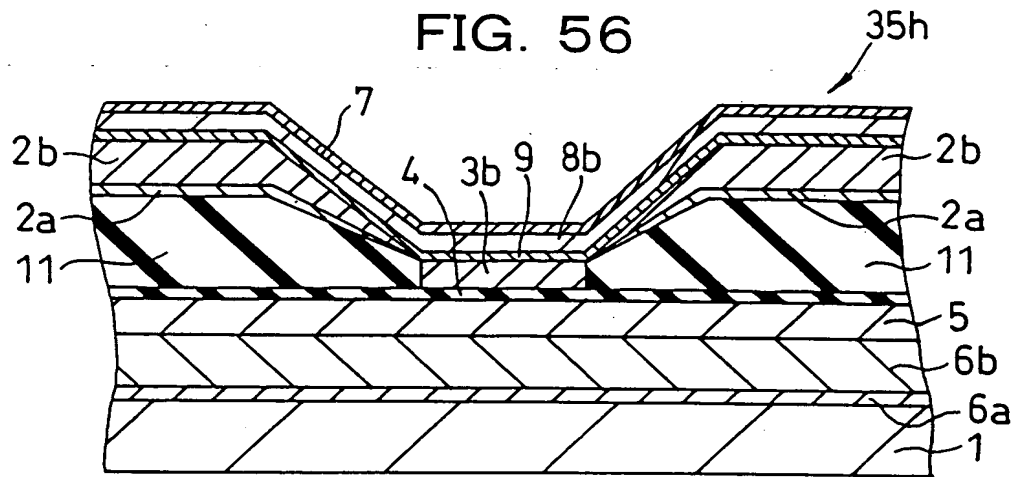


FIG. 57

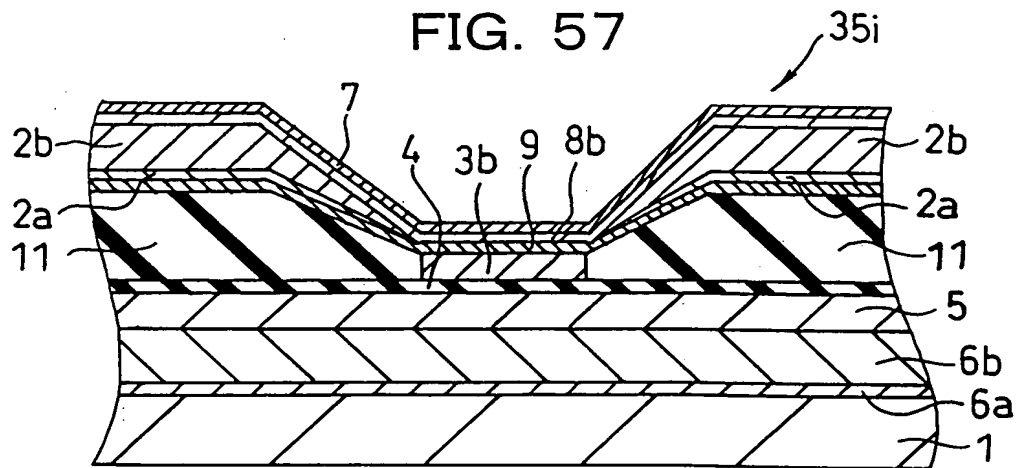


FIG. 58

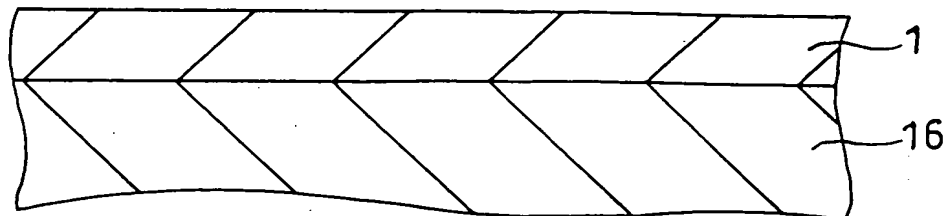


FIG. 59

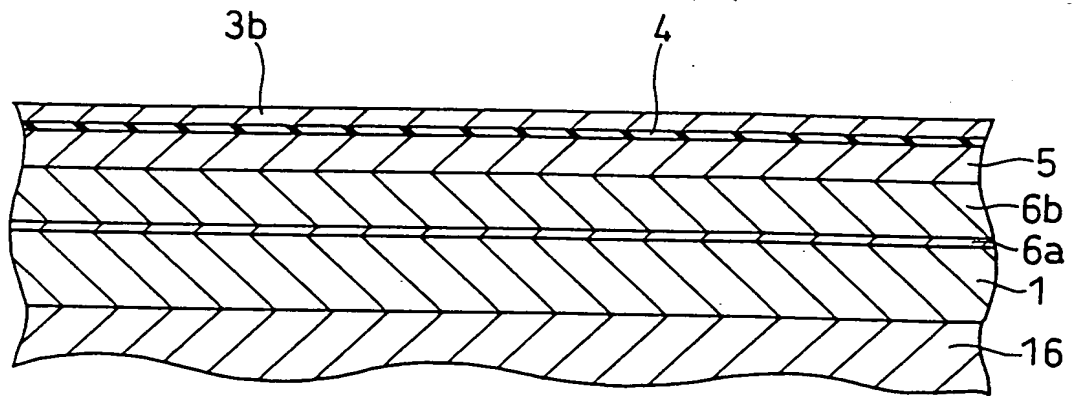


FIG. 60

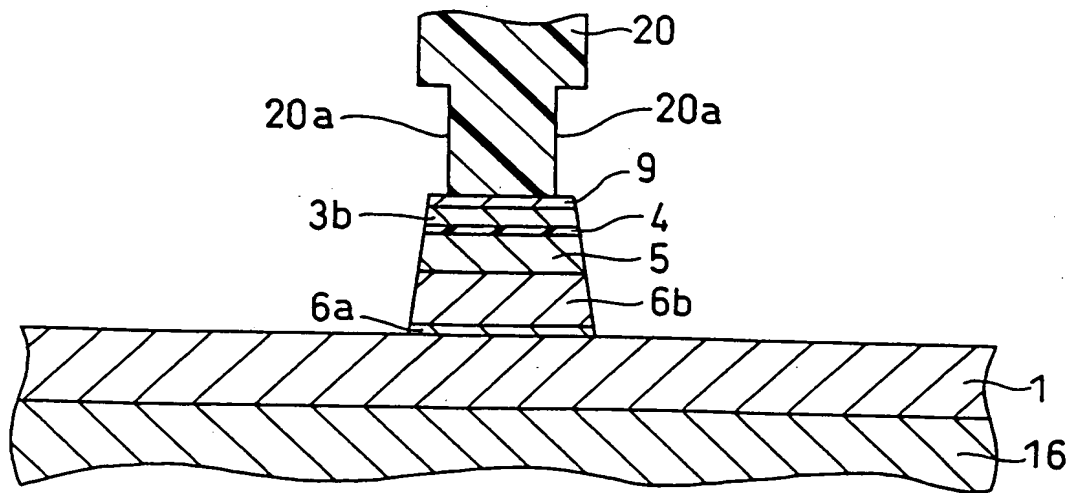


FIG. 61

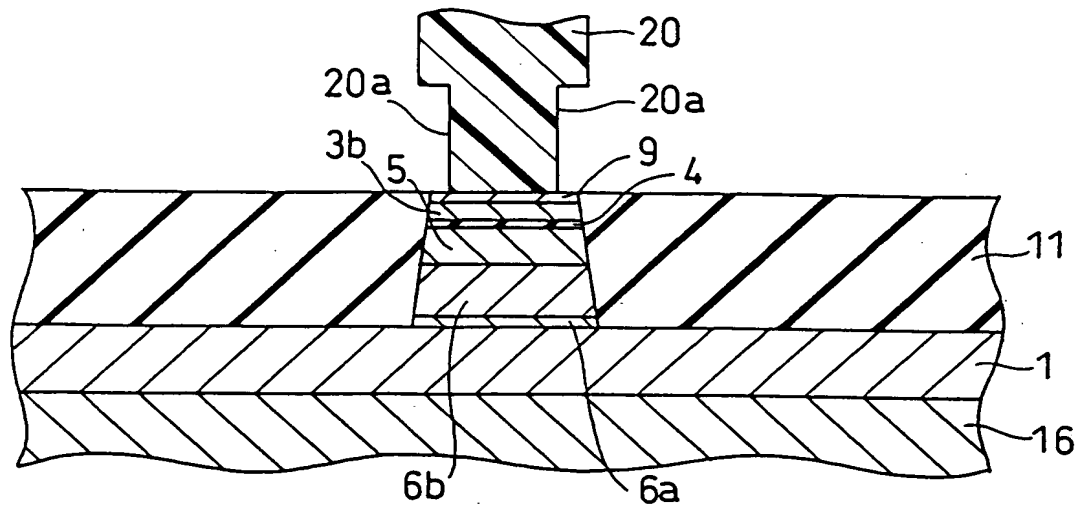


FIG. 62

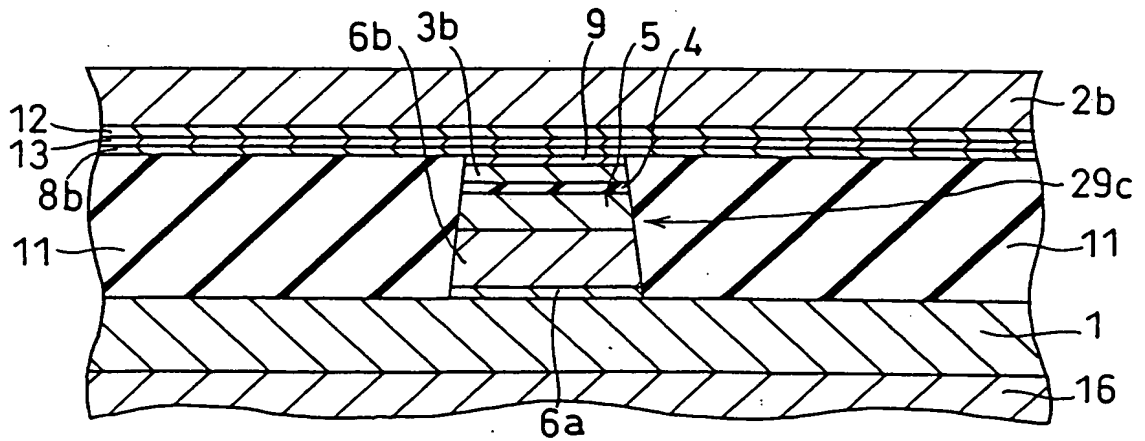


FIG. 63

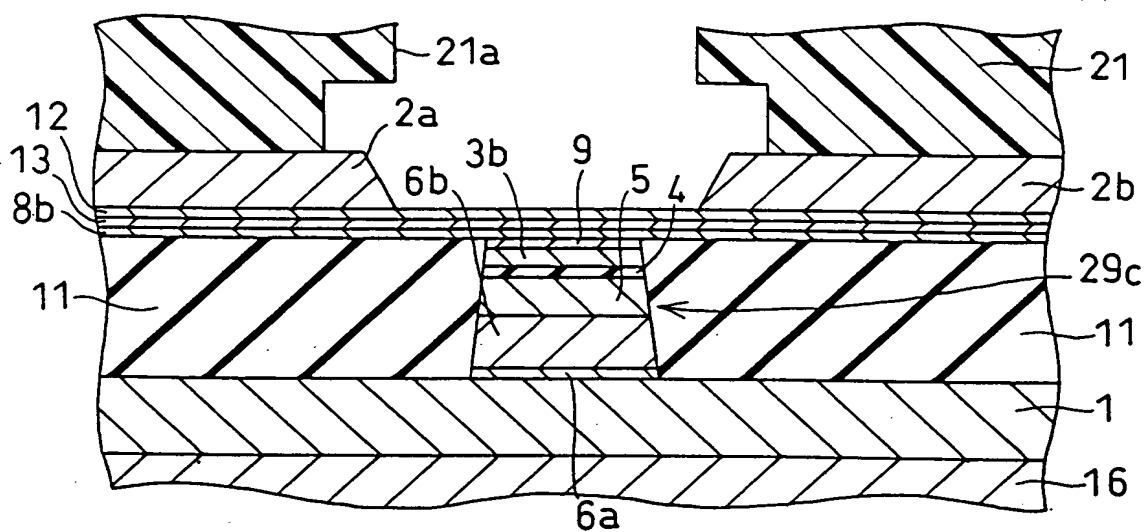
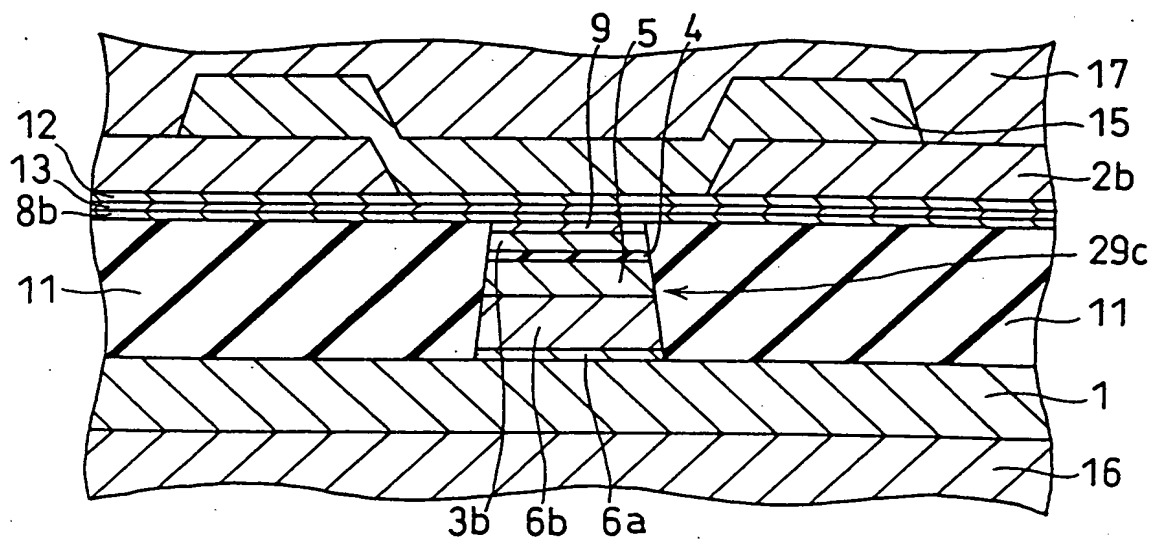
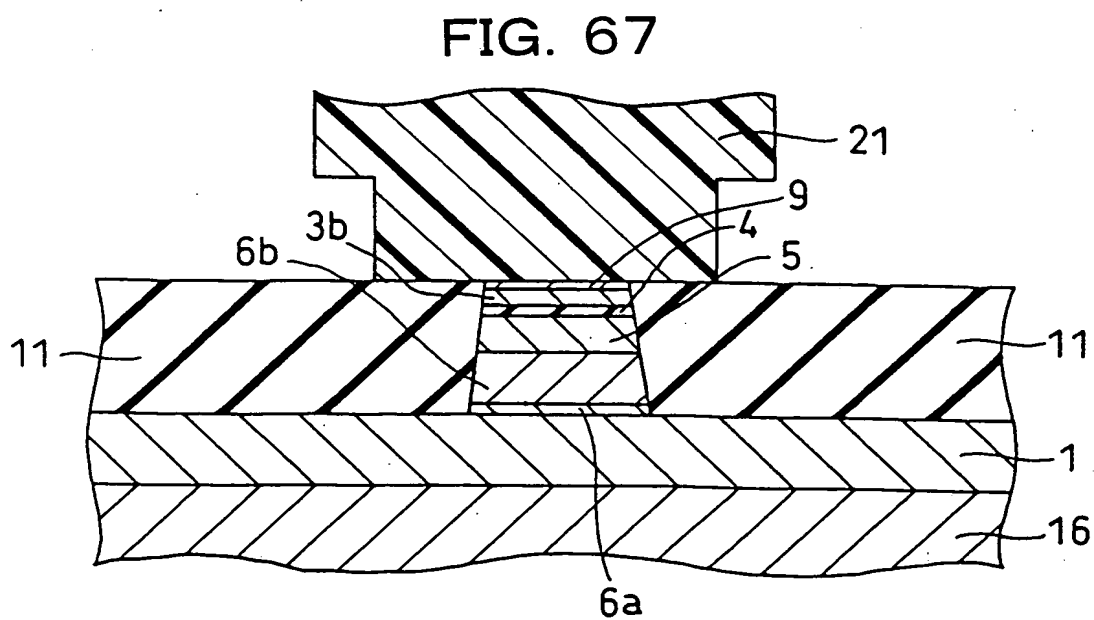
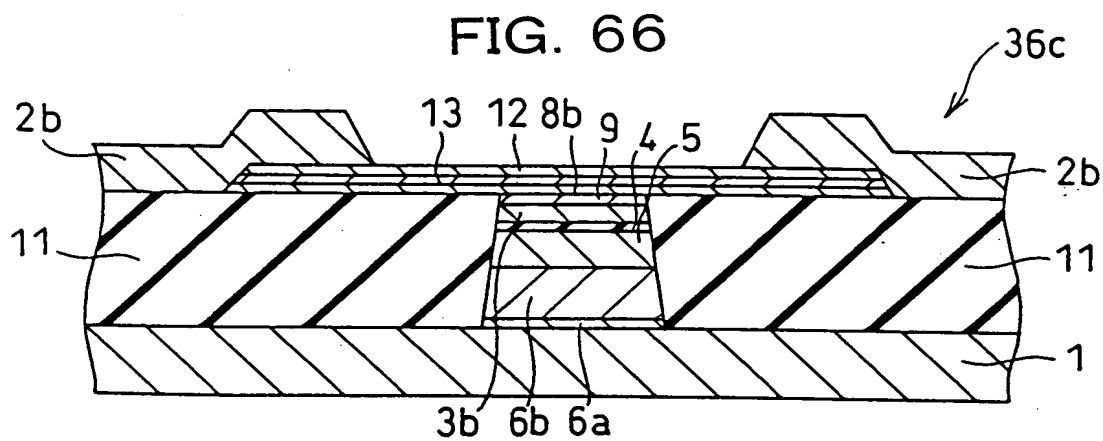
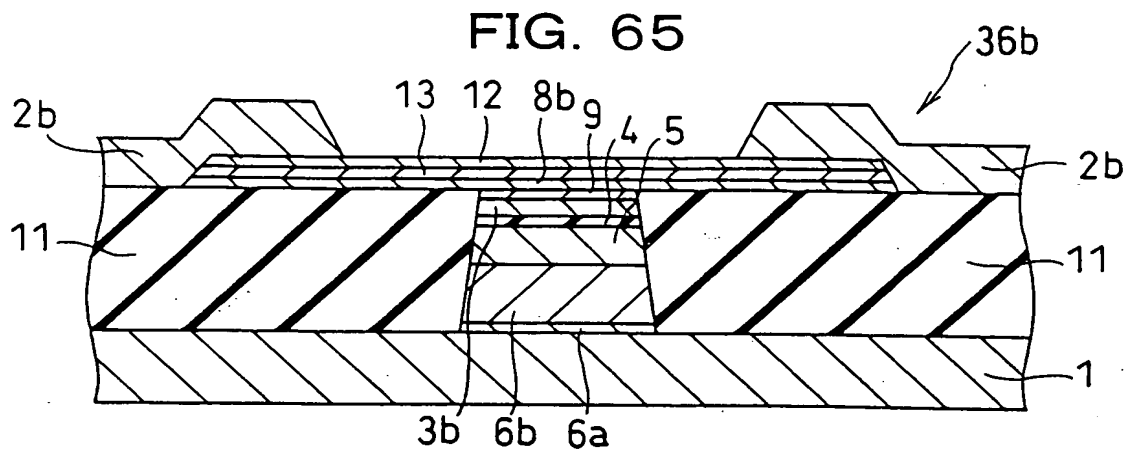


FIG. 64





[illegible]

FIG. 70

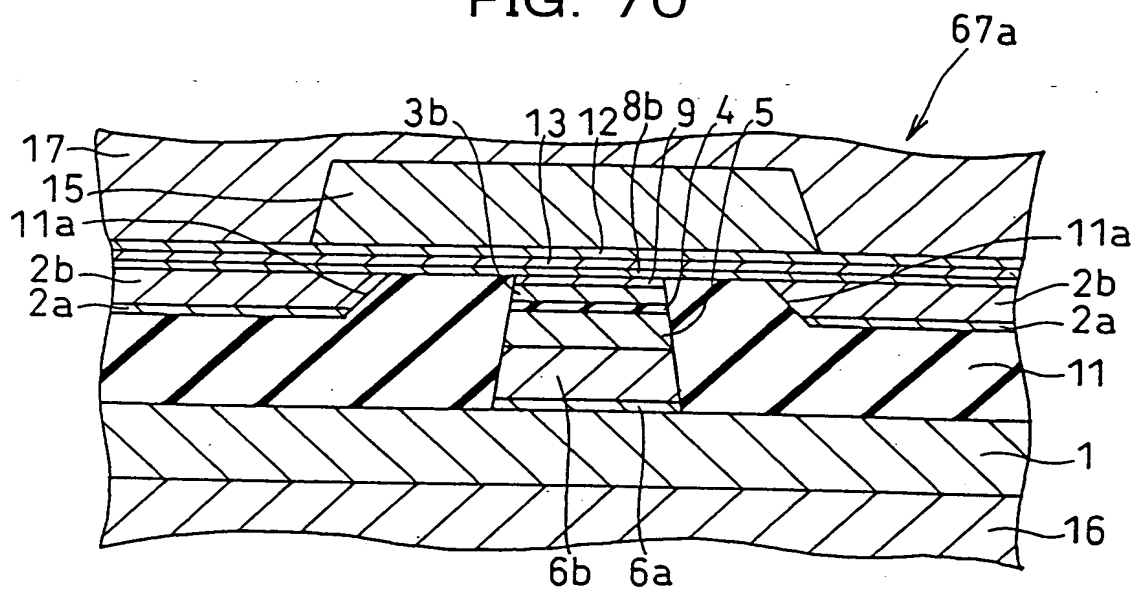


FIG. 71

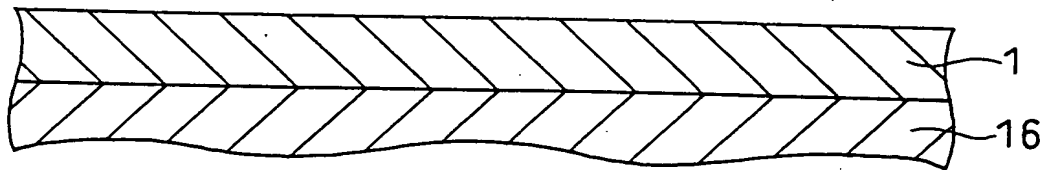


FIG. 72

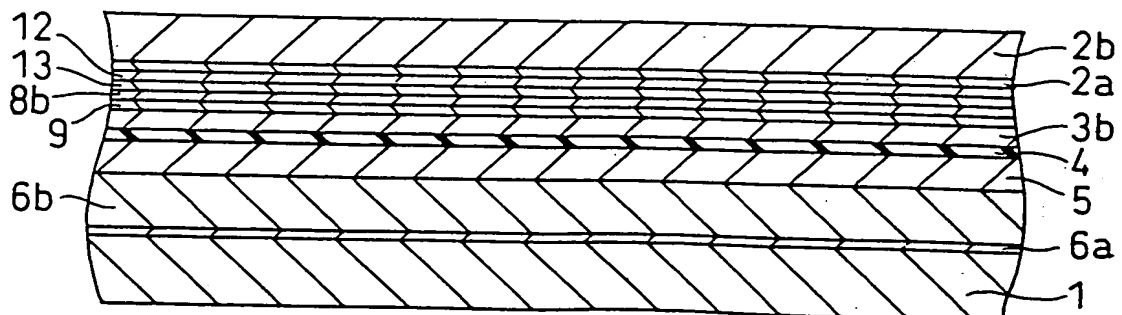


FIG. 73

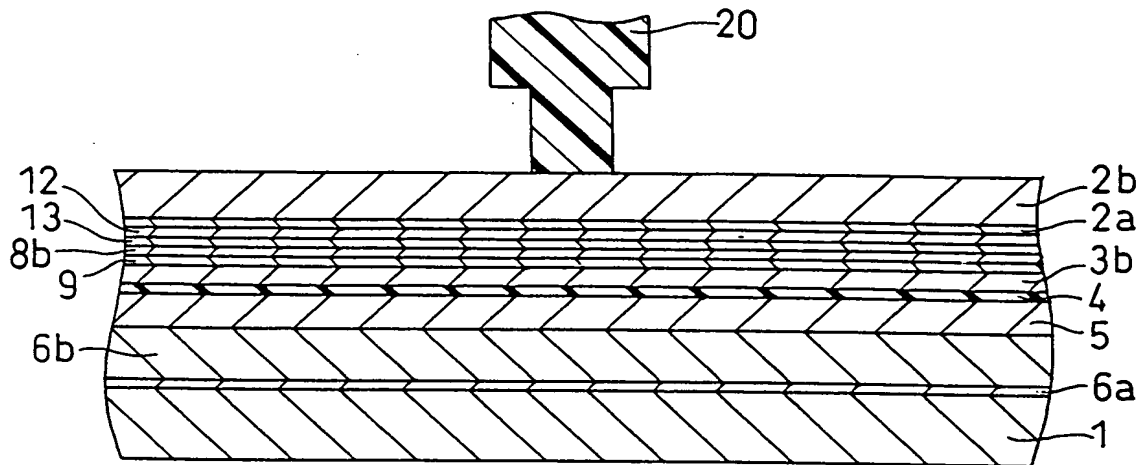


FIG. 74

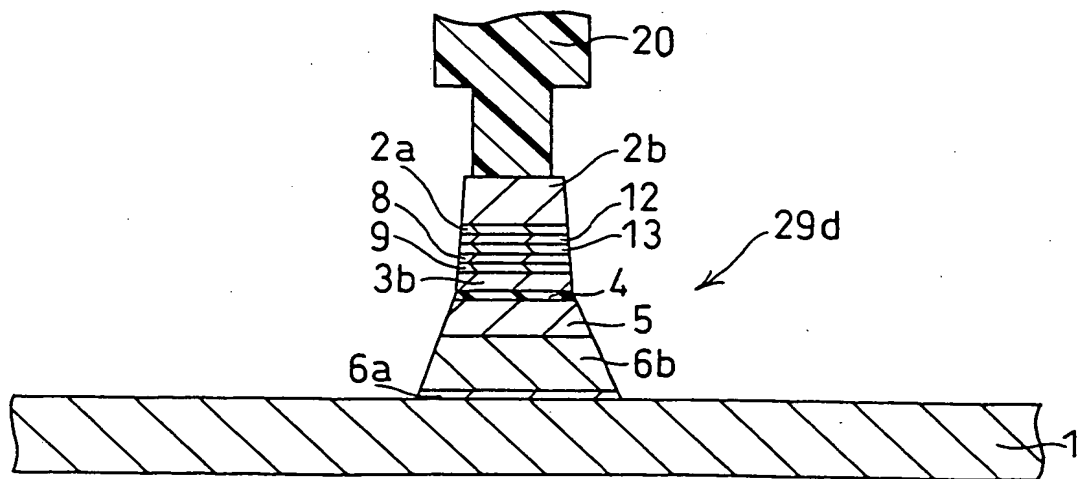


FIG. 75

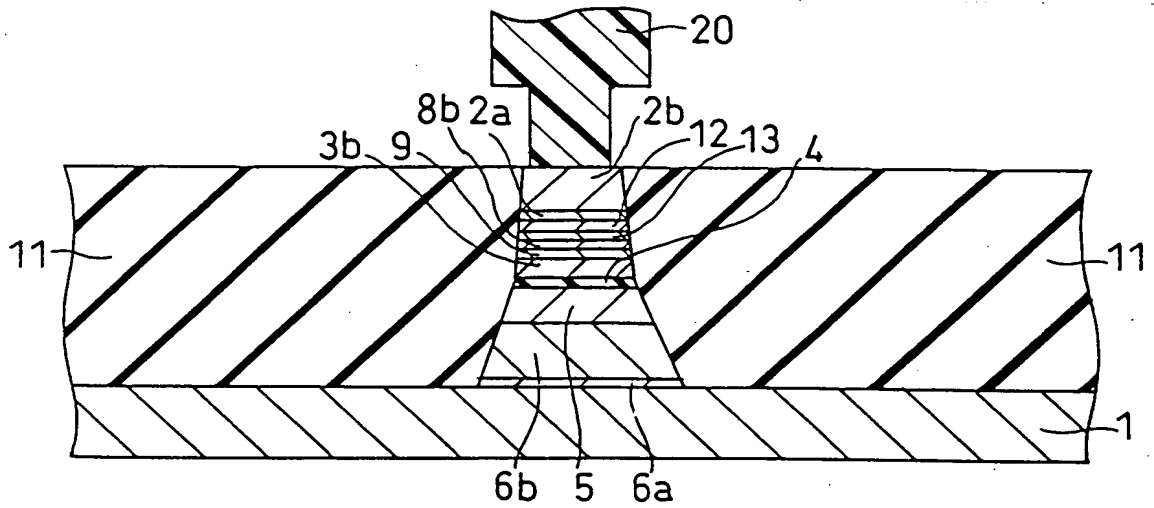


FIG. 76

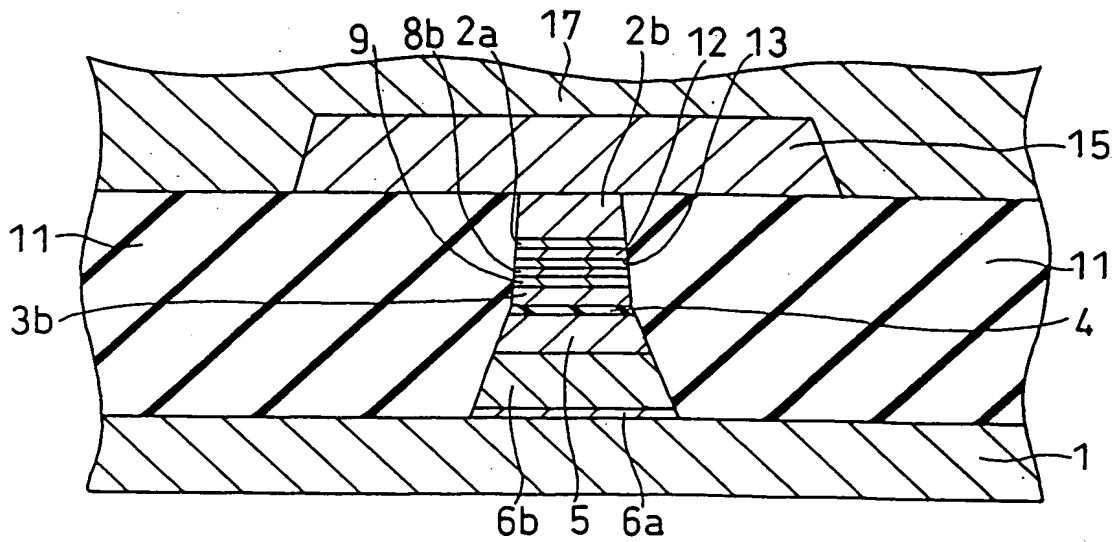


FIG. 77

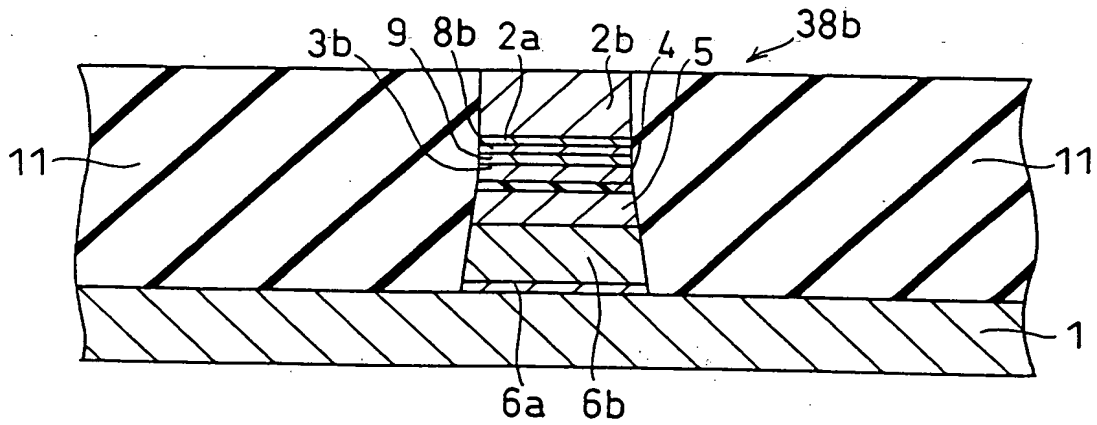


FIG. 78

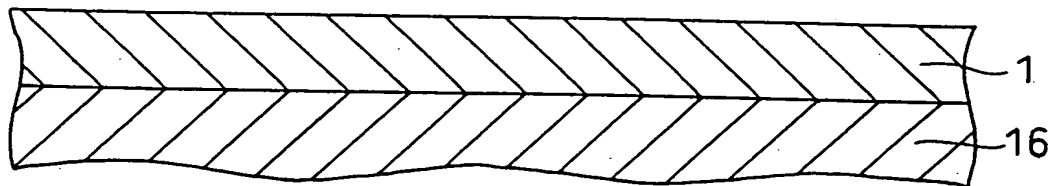


FIG. 79

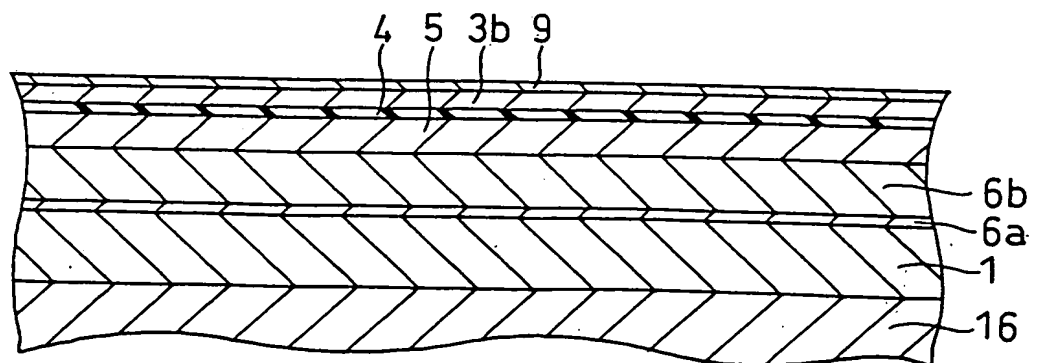


FIG. 80

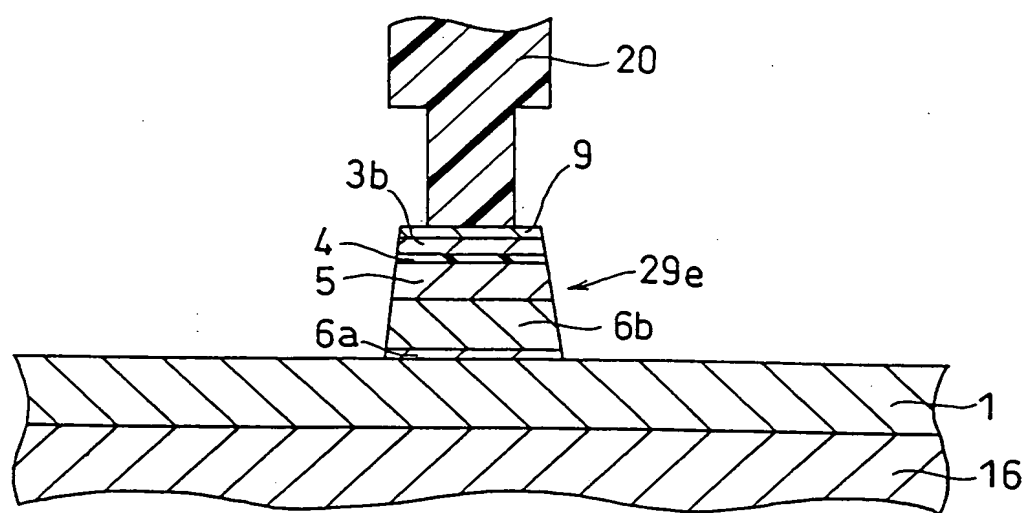


FIG. 81

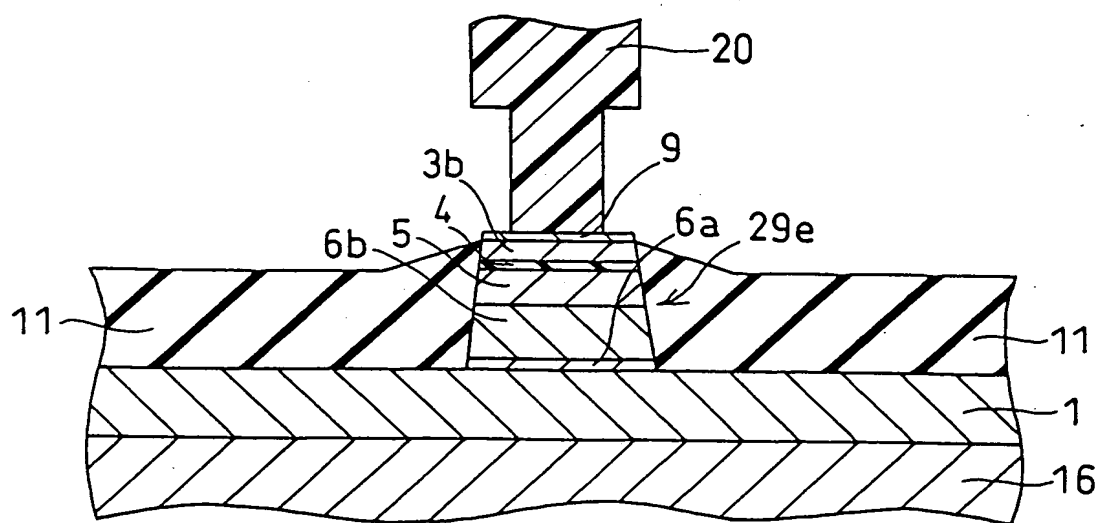


FIG. 82

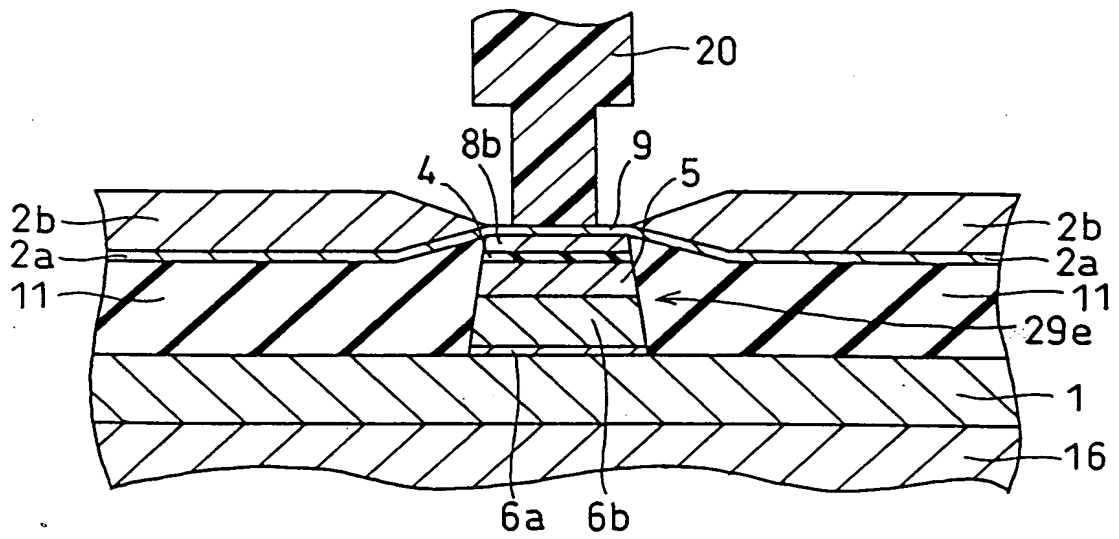


FIG. 83

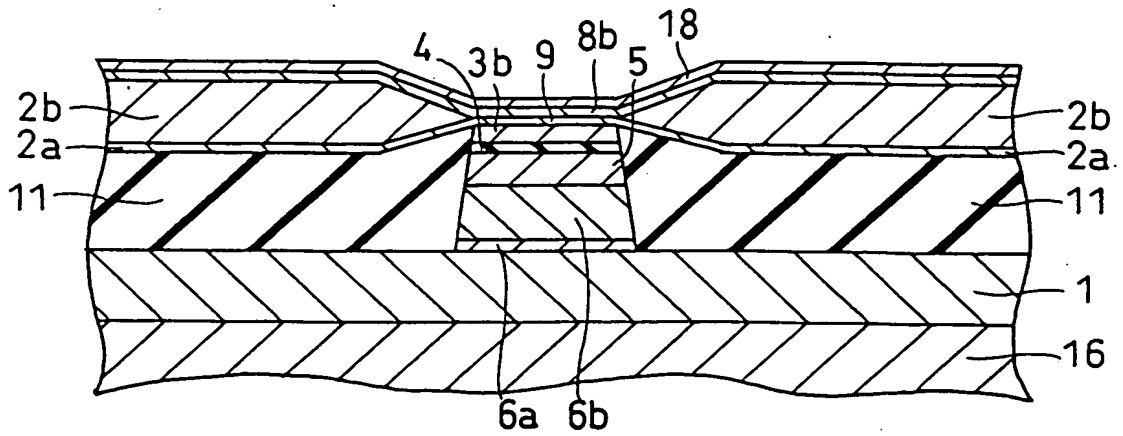


FIG. 84

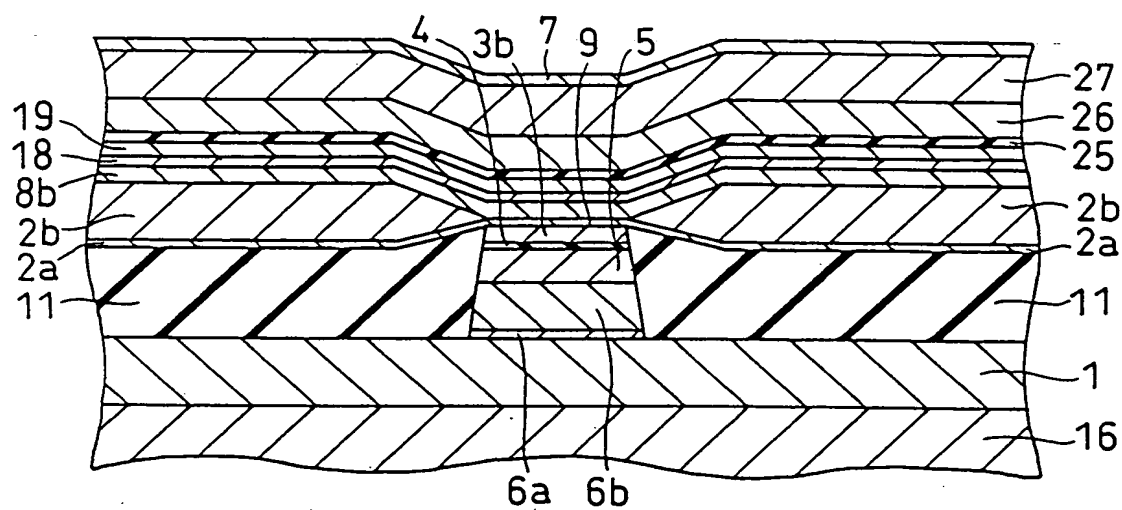


FIG. 85

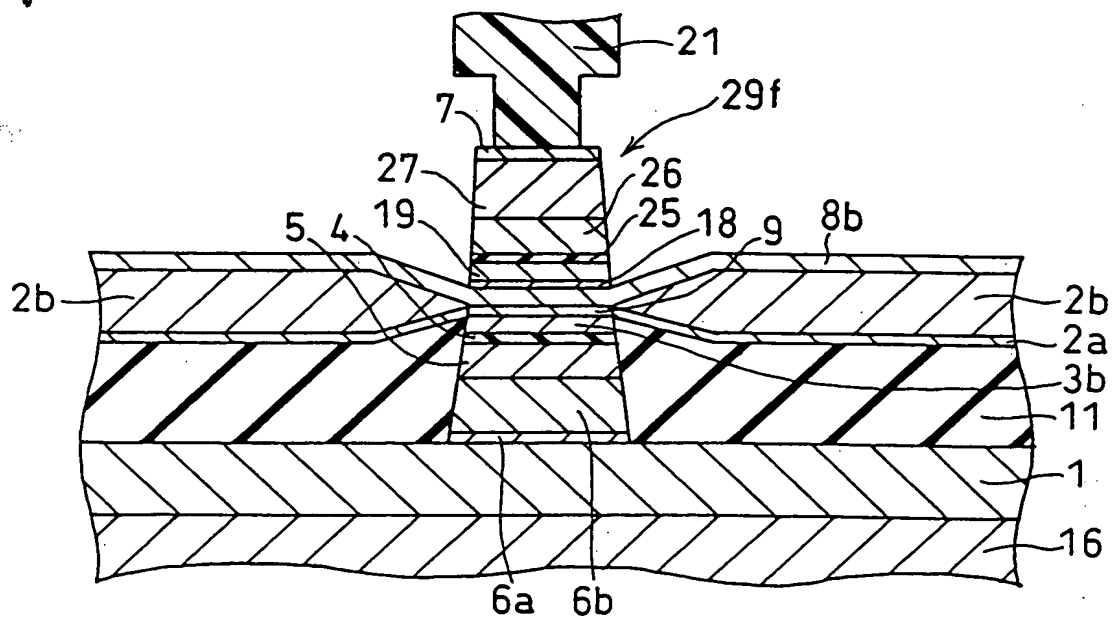


FIG. 86

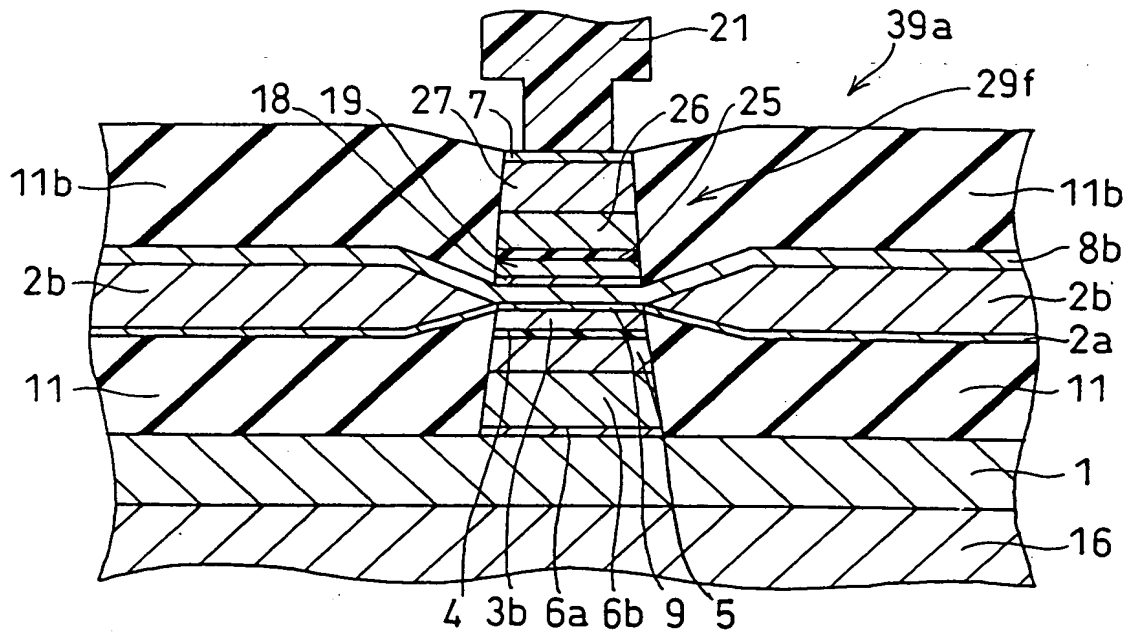


FIG. 87

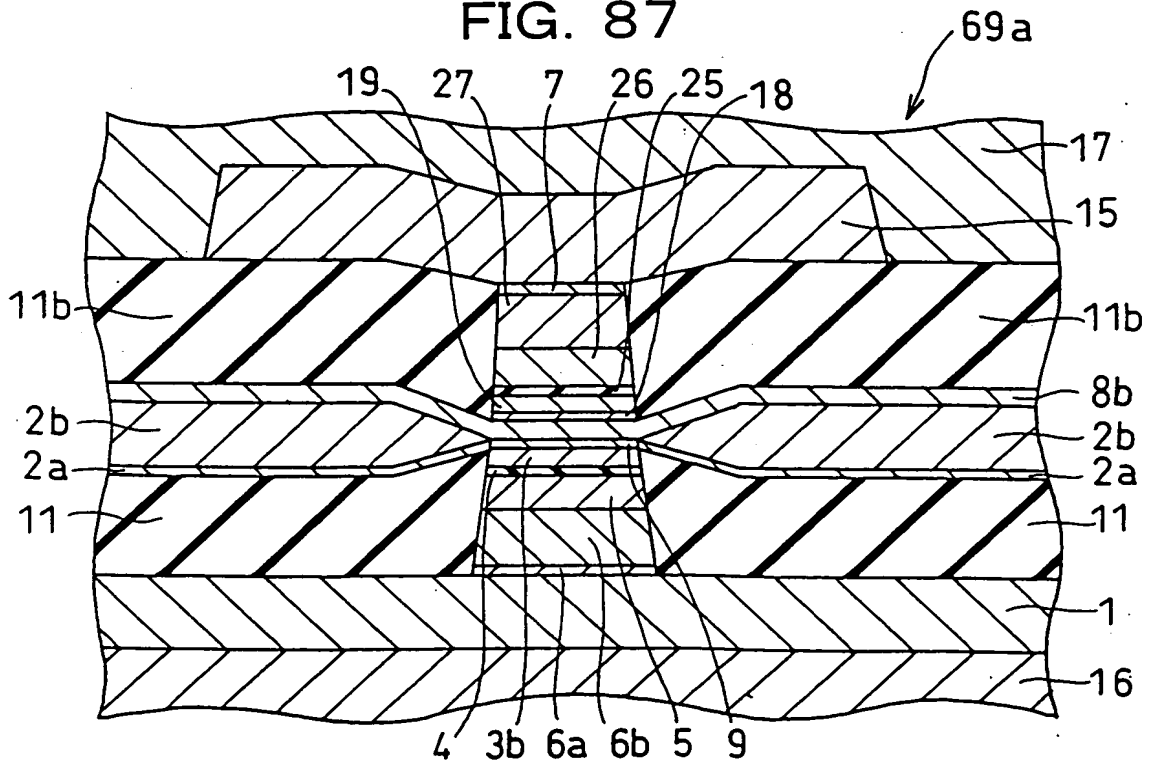


FIG. 88

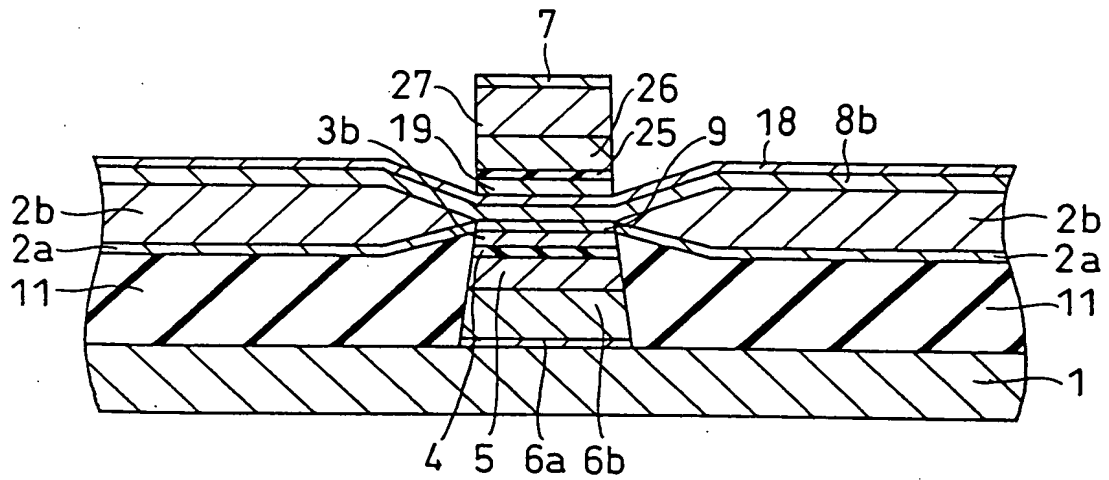
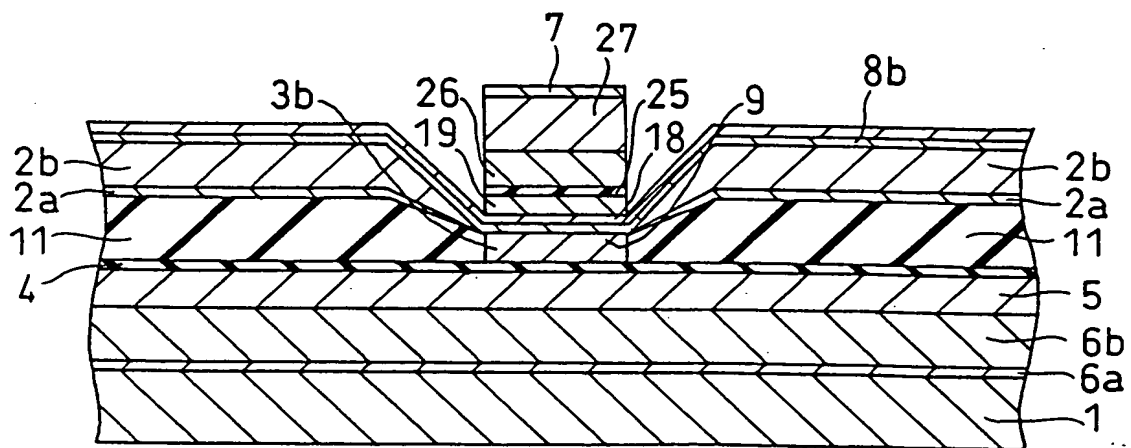


FIG. 89



[illegible]

FIG. 92

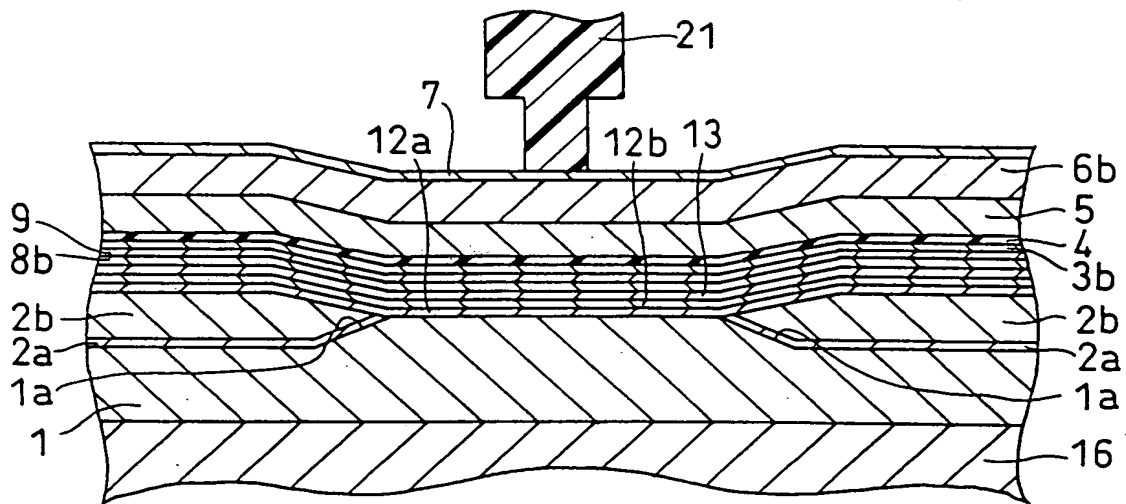


FIG. 93

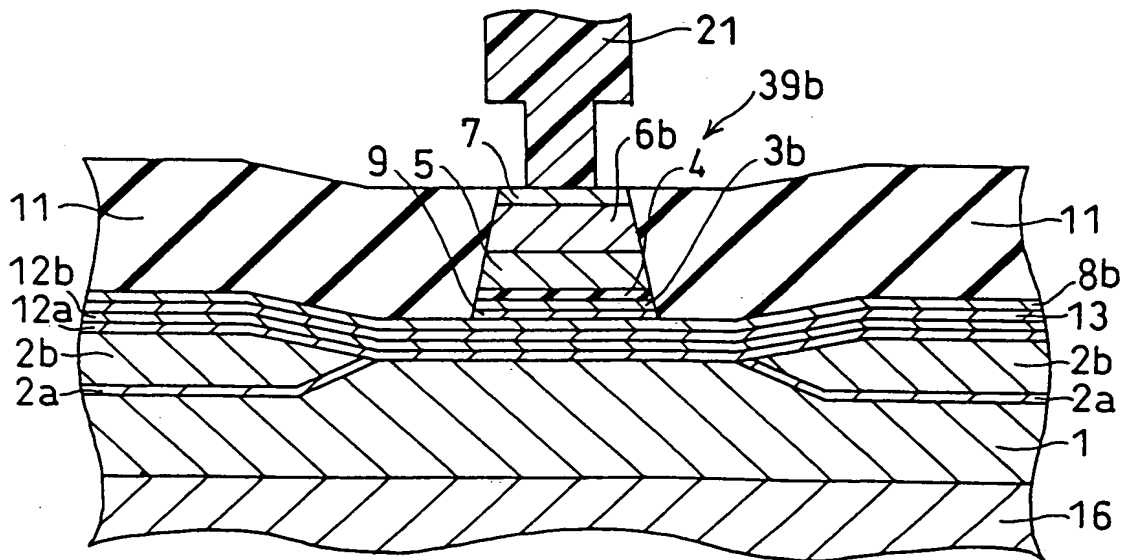


FIG. 96

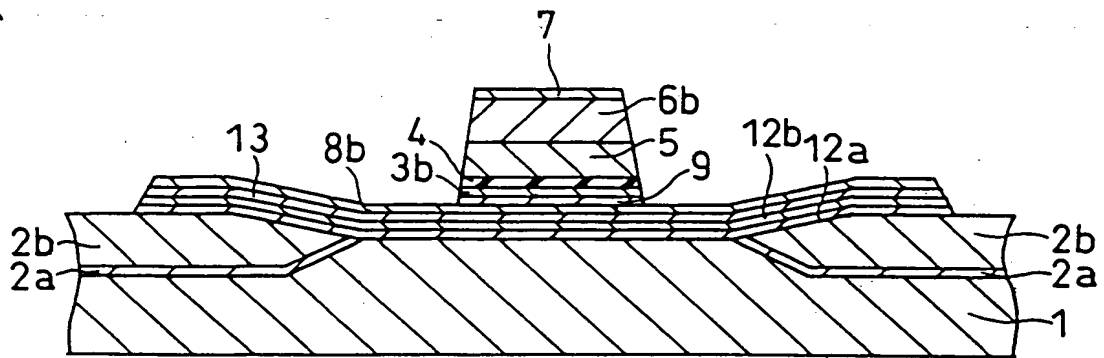


FIG. 97

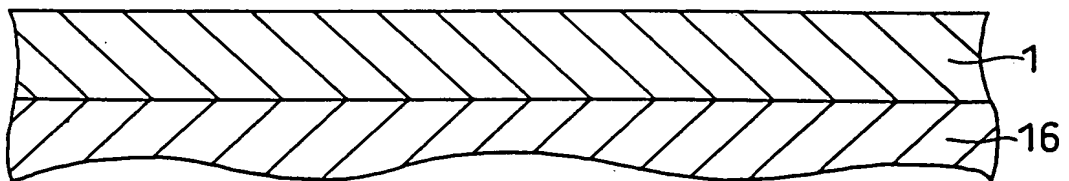


FIG. 98

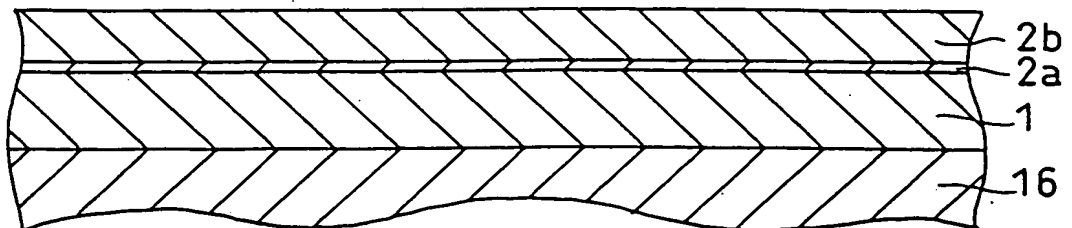


FIG. 99

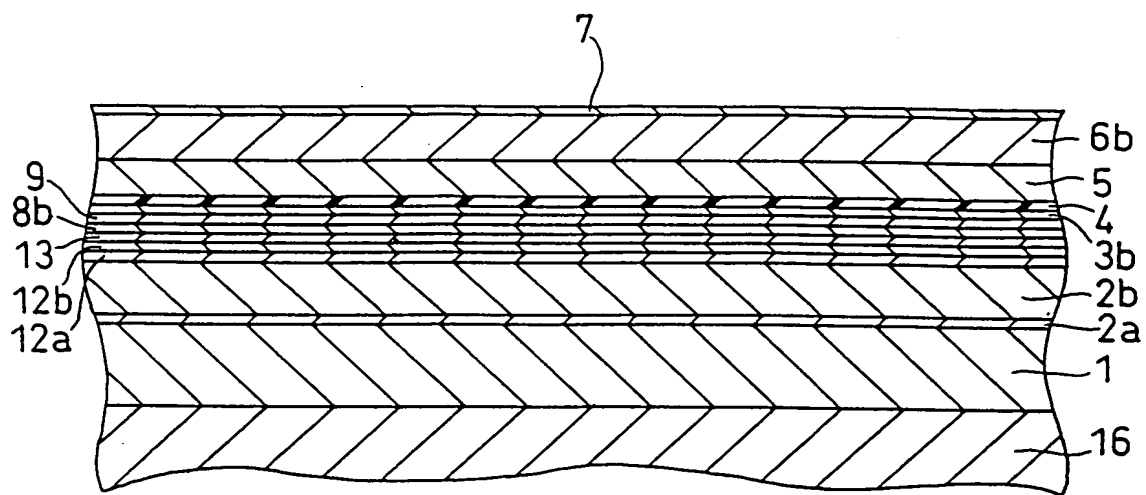


FIG. 100

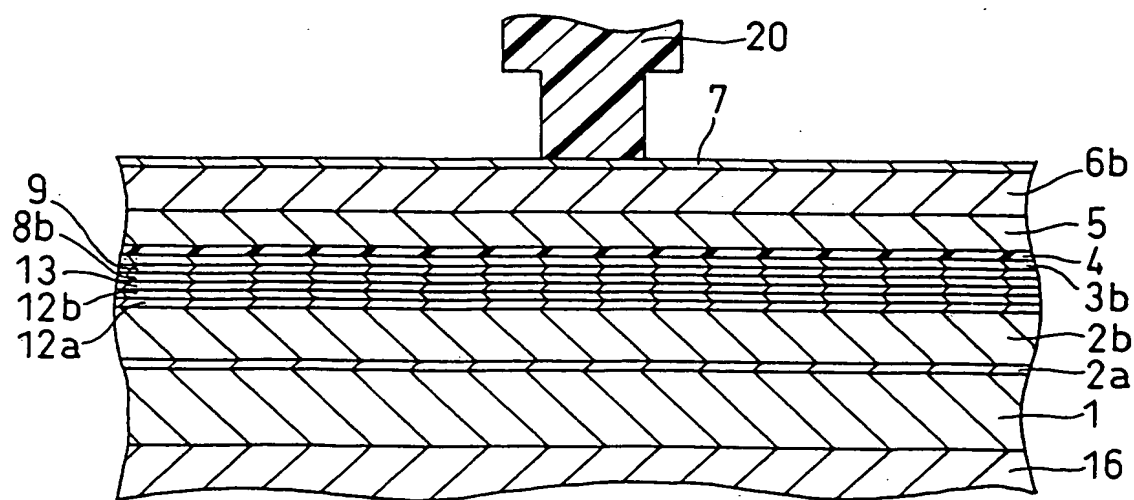


FIG. 101

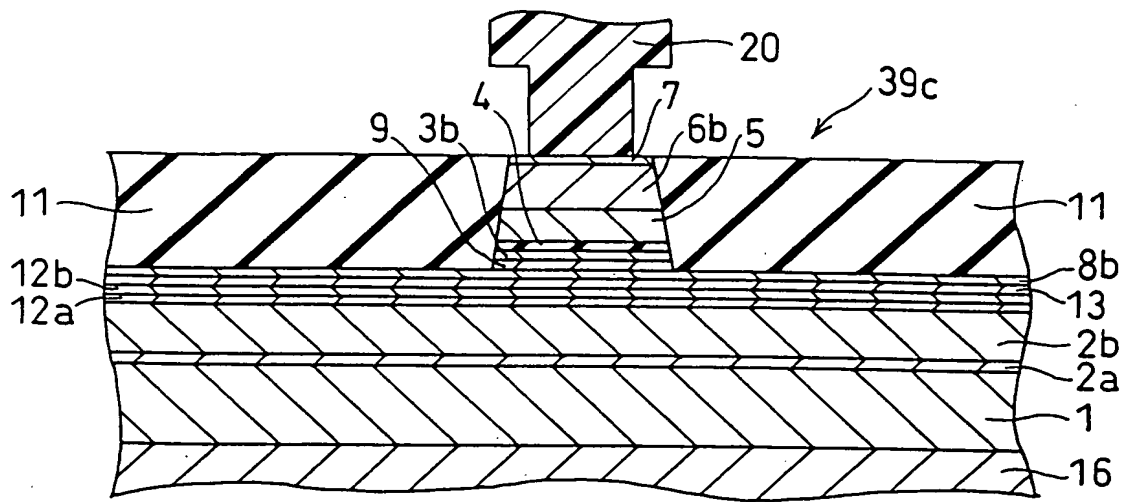


FIG. 102

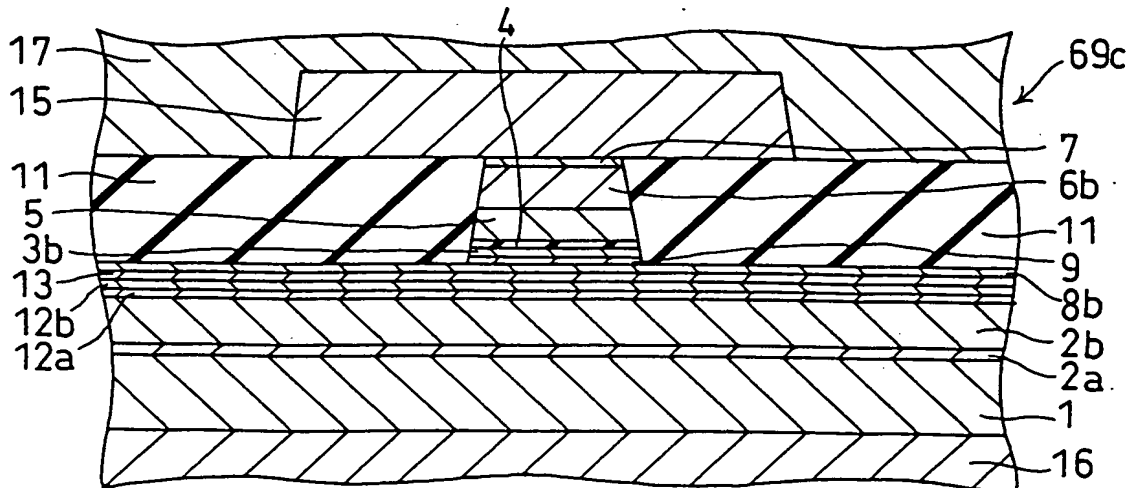


FIG. 103

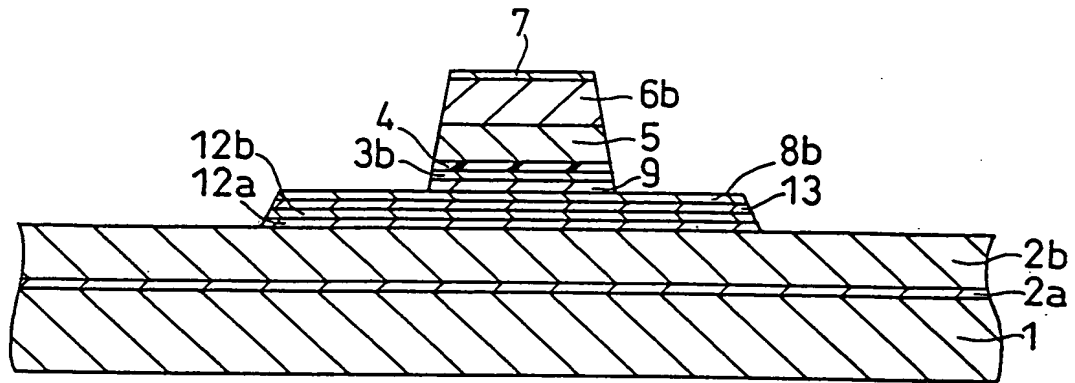


FIG. 104

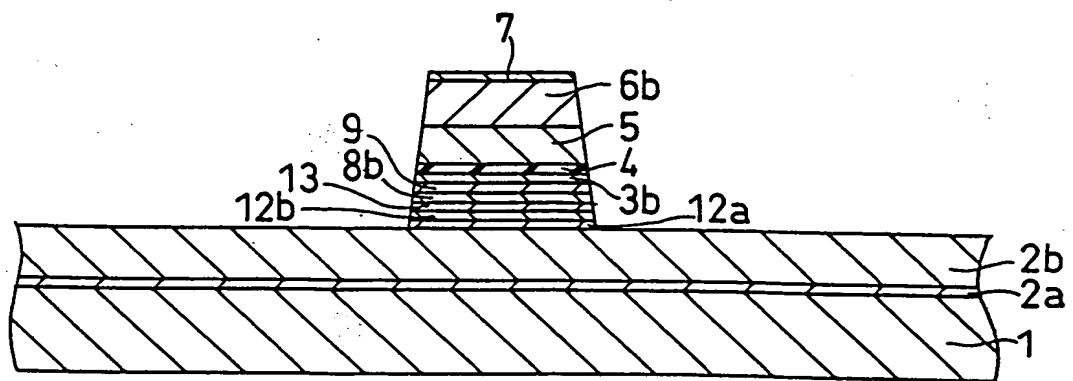


FIG. 105

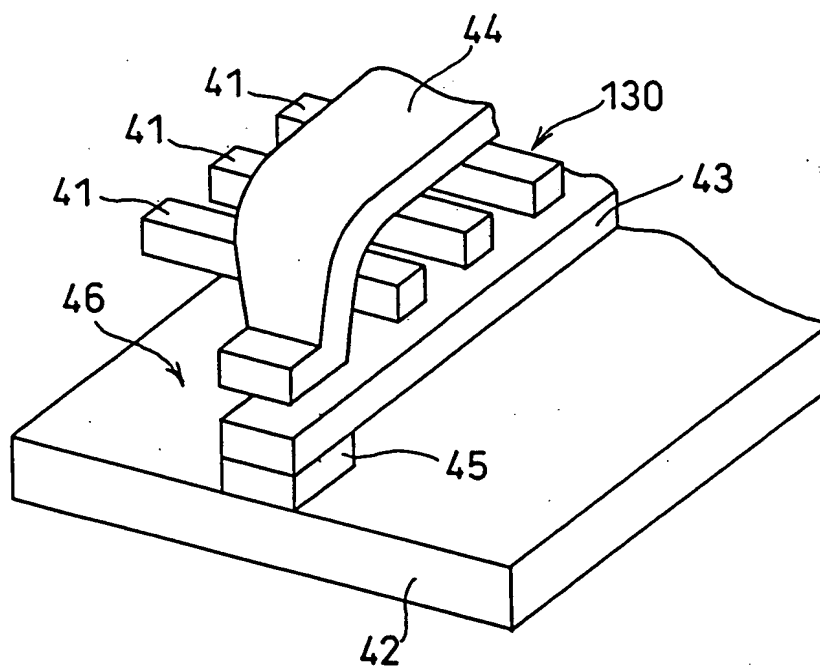


FIG. 106

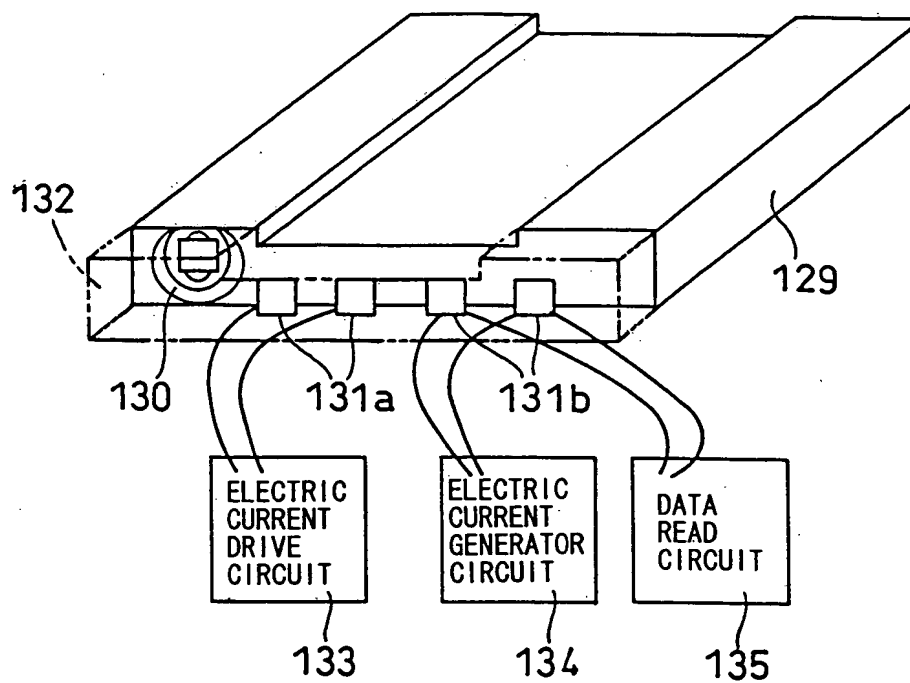


FIG. 107

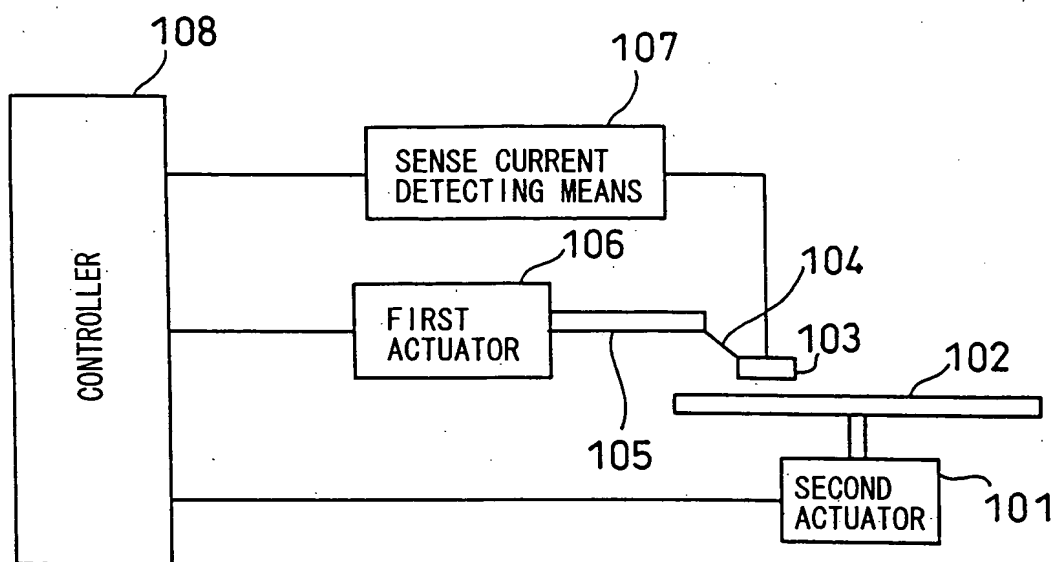


FIG. 108

